DIFFERENT MATHEMATICAL RELATIONS WITH CMOS VLSI CIRCUITS

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ABSTRACT

In this paper, Analog VLSI CMOS circuits that implements different mathematical functions, equations, or relations such as "Addition, Subtraction, Multiplier, Quadratic, Square Root, Linear, and Hyperbolic Tangent relations" with limited and wide range variations are presented. These relations and functions are useful for analog neural network hardware and analog signal processing implementation.

Keywords: CMOS VLSI implementation, analog circuit, mathematical equations, neural network, spice simulation

INTRODUCTION

Although high performance bipolar transistors multipliers have been available for some time, the CMOS multiplier implementation is still a challenging subject especially for low-voltage/low-power circuit design (Han & Sinencio, 1998). The transistors can be biased in Strong Inversion and Weak Inversion. Weak inversion is widely used in such circuits, but often it leads to low precision (Prodanov & Green, 1997). Functions such as "Addition, Subtraction, Multiplier, Quadratic, Square Root, Linear, Hyperbolic Tangent relations" are profoundly required and are the key computational elements in analog signal processing "Mixers, Modulator, *etc*…" and analog neural networks. The massively parallel analog systems have demonstrated potential for solving a wide range of difficult problems, and thus analog computing techniques have become more widespread (Saxena & Clark, 1994). Analog neural networks are heavy parallel analog systems, which are used and are demonstrated in solving a wide range of real world problems (Annema, 1995). Multi Layer Perceptron MLP trained by the back propagation algorithm needs neurons connected to synapses. Each synapse needs a multiplier to multiply the input times the weight (Bo *et al*., 1999; Chiblè, 1997; Chiblè, 2000; Valle *et al*., 1996; Saxena & Clark, 1994; Ghandour & Chiblè, 2007) and also needs another multiplier to multiply the input times the error transmitted from the neuron "tutorial of CMOS Circuits "trans-conductance multiplier" is presented in (Han & Sinencio, 1998)". Each neuron needs an addition relation "that adds all its inputs", non-linear relation "between the input and the output of the neuron" such as hyperbolic tangent, difference function "that needs the difference between the output and the target of the neuron", derivative relation "that compute the derivative of the output". The analog neural networks system may contain tenth of thousands of these relations, because of that the area and the power consumption of the

CMOS VLSI implementation must be as small as possible. The purpose of this paper is to present circuits that implement these mathematical relations or equations.

In this paper the following sections are presented: Quadratic relation, Wide range quadratic relation, Square root-linear and difference relations, Parametric Wide-Small range linear and Parametric Wide quadratic relations, Wide Range "Linear & Quadratic" Multiplier, Simulation Results, and finally the conclusions.

QUADRATIC RELATION

Figure 1 shows three transistors that create a quadratic relation between the current I_1 and the input voltage V_w. It is a simple circuit used to convert voltage into current.

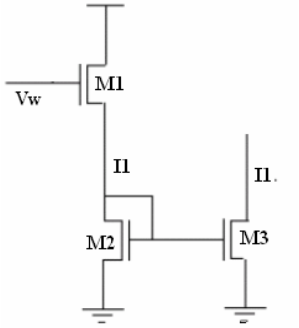

Figure 1. Quadratic relation circuit.

If the transistor M1 works in strong inversion *(i.e.* condition (A) must be verified) and saturation region (*i.e.* condition (B) must be verified), the current I_1 (channel length modulation is neglected) is given by (Vittoz, 1994):

$I_1 = \frac{\beta_1}{2n} \times (V_w - nV_1 - V_{TH1})^2$	$(A): ....V_w - nV_1 > V_{TH1}$ $(B): ....V_{dd} - V_1 \geq V_w - nV_1 - V_{TH1}$

where $\beta_1 = \mu_1 \times C_{ox} (W/L)_1$ is the transfer parameter, n is the slope factor usually smaller than 2 which tends to 1 for very large values of the gate voltage (Vittoz, 1994); μ_1 is the carrier mobility of the transistor M1, C_{ox} is the gate oxide capacitor per unit area, $(W/L)_1$ is the channel width-to-length ratio of M1, V_{TH1} is the gate threshold voltage of M1, and V_1 is the source voltage of M1. V_{dd} value depends on the type of technology; it may be either 5V or 3.3V.

Please note that the above equation is the simplified expression of the transistor model presented in (Vittoz, 1994), but in fact if the gate source voltage equals to the threshold voltage, the drain current is equal to a small current I_s (called the specific current) and not to zero as in the above equation. While if the gate source voltage is lower than the threshold voltage, the transistor is in weak inversion and the drain current is less than I_s and it has an exponential relation with respect to the gate source voltage. I_s value depends on (W/L) values. The dimensions of the transistors M1 and M2 can be designed in a way as to decrease the specific current value.

The current that passes in M1 is equal to the current that circulates through M2. If the transistor M2 works in strong inversion ($V_1 > V_{TH2}$) and it is always in saturation because its drain-gate voltage is zero. Then the current of M2 (channel length modulation is neglected) is given by:

$$I_1 = \frac{\beta_2}{2n} \times (V_1 - V_{TH2})^2 \quad \rightarrow \quad V_1 = V_{TH2} + \sqrt{2n \frac{I_1}{\beta_2}}$$

By substituting the value of V_1 in the previous equation of I_1 current of transistor M1, the equation becomes as follows:

$I_1 = \frac{\beta_n}{2n} \times (V_w - V_{0n})^2$	Equation 1

where $V_{on} = V_{TH1} + n\, V_{TH2}$; β_n is given by:

$$\frac{1}{\sqrt{\beta_n}} = \frac{1}{\sqrt{\beta_1}} + n \frac{1}{\sqrt{\beta_2}}$$

Conditions (A) and (B) must be verified. The condition (B) is always satisfied, because it can be rewritten as follows:

$$nV_1 \geq V_1 + V_w - V_{dd} - V_{TH1}$$

If $V_w = 0V$ the condition (B) is satisfied and if ($V_w = V_{dd}$) it is also satisfied. By substituting V_1 in the condition (A), we obtain the following condition:

$$V_w > V_{0n} + n\sqrt{2n\, I_1 / \beta_2}$$

If $I_1=0$ Then $V_w = V_{on}$. In conclusion, the condition (A) is satisfied if the weight voltage is greater than V_{on}.

WIDE RANGE QUADRATIC RELATION

To work with larger V_w, we add five transistors to Figure 1 as shown in Figure 2 that creates a quadratic relation between the current I_2 and the input voltage V_w.

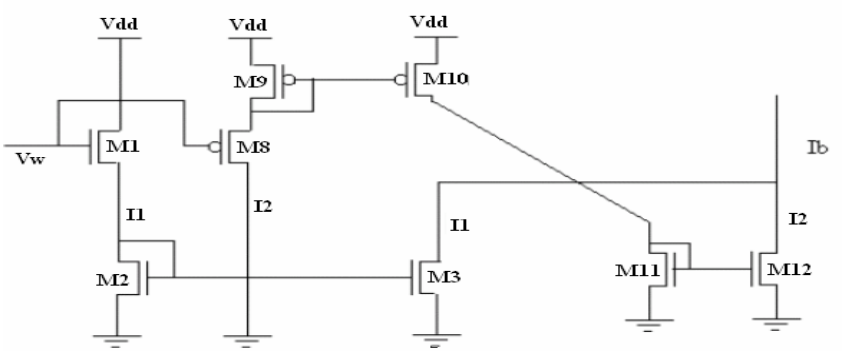

Figure 2. Wide range quadratic relation circuit ($I_b = I_1 + I_2$).

A similar analysis to obtain the output current I_2 can be performed:

$I_2 = \frac{\beta_p}{2n} \times (V_w - V_{0p})^2$	Equation 2

where V_{op} and ß$_p$ are given by:

$$V_{0p} = n^2 V_{dd} - nV_{TH9} - V_{TH8} \quad \& \quad \frac{1}{\sqrt{\beta_p}} = \frac{1}{\sqrt{\beta_8}} + n\frac{1}{\sqrt{\beta_9}}$$

The current I_b is given by (I_1+I_2):

$$I_b = \begin{cases} I_1 \to V_{on} < V_w < V_{dd} \\ I_2 \to 0 < V_w < V_{0p} \end{cases}$$

Note that, I_1 and I_2 have the same sign. By substituting the value of I_1 and I_2 in the above equation, we obtain:

$$I_b = \begin{cases} \frac{\beta_n}{2n} \times (V_w - V_{0n})^2 \to V_{on} < V_w < V_{dd} \\ \frac{\beta_p}{2n} \times (V_w - V_{0p})^2 \to 0 < V_w < V_{0p} \end{cases}$$

By designing the transistors' dimensions, we can assume that $\beta_p = \beta_n = \beta_0$ and $V_{0p} = V_{0n} = V_0$. Then I_b is given as follows:

$I_b = \frac{\beta_0}{2n} \times (V_w - V_0)^2 \to 0 < V_w < V_{dd}$	Equation 3

Note that I_1 & I_2 have the same sign in Figure 2. To make the signs different between I_1 & I_2, Figure 3 is proposed.

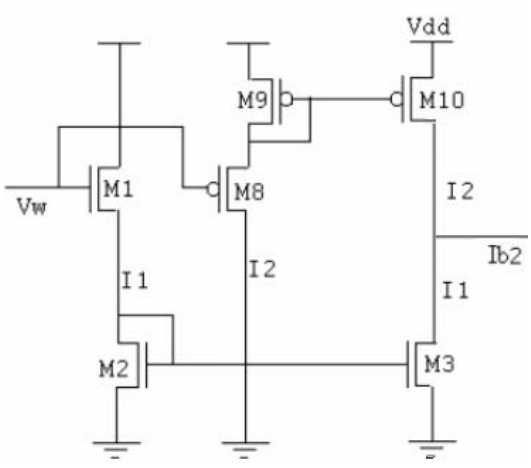

Figure 3. Difference between I_2 & I_1.

The equation of I_{b2} is given by:

$$I_{b2} = \begin{cases} I_1 \to V_o < V_w < V_{dd} \\ -I_2 \to 0 < V_w < V_0 \end{cases} = \begin{cases} \frac{\beta_0}{2n} \times (V_w - V_0)^2 \to V_o < V_w < V_{dd} \\ -\frac{\beta_0}{2n} \times (V_w - V_0)^2 \to 0 < V_w < V_0 \end{cases}$$

The above equation can be written in the following mode:

$I_{b2} = \frac{\beta_0}{2n} \times (V_w - V_0)\lvert V_w - V_0 \rvert \to 0 < V_w < V_{dd}$	Equation 4

SQUARE ROOT, SMALL RANGE LINEAR AND DIFFERENCE RELATIONS

The following circuit is famous and well known and it is called as OTA operational transconductance amplifier. It can be used to produce a linear relation or a square root relation between the output current I_{out} and the input current I_b. The relation type depends on the maximum input current and on the dimensions of the transistors M4 and M5 (Valle *et al*., 1996; Vittoz, 1994; Mead, 1989). V_{in} is the input voltage and V_{ref} equals to V_{dd} /2.

If the maximum input current I_b, and the dimensions of the transistors M4 and M5 are designed in order to work in strong inversion, then the output current I_{out} is given by (Chiblè, 2000; Chiblè, 2003a; Chiblè, 2003b):

$$I_{out} = \sqrt{\frac{\beta_{5,4}}{n}} \sqrt{I_b} (V_{in} - V_{ref}) \sqrt{1 - \frac{(V_{in} - V_{ref})^2}{\frac{4nI_b}{\beta_{5,4}}}}$$

Where $ß_{5,4}$ is the relative transfer parameter of M4 and M5. If $|V_{in} - V_{ref}| << \sqrt{4nI_b / \beta_{5,4}}$ or V_{in} varies in the range $[V_{ref} - \sqrt{4nI_b / \beta_{5,4}} : V_{ref} + \sqrt{4nI_b / \beta_{5,4}}]$, then the last equation can be rewritten as follows:

$I_{out} = \sqrt{\frac{\beta_{5,4}}{n}} \sqrt{I_b} (V_{in} - V_{ref})$	Equation 5

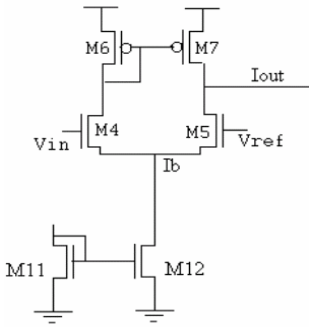

Figure 4. Square root or linear relation circuit.

The relation between I_{out} & I_b is a square root and the relation between I_{out} & V_{in} is linear. If the maximum input current I_b, and the dimensions of the transistors M4 and M5 are design in order to work in weak inversion, then the output current I_{out} is given by (Mead, 1989):

$$I_{out} = I_b Tanh\left(\frac{V_{in} - V_{ref}}{2nV_t}\right)$$

If $|V_{in} - V_{ref}| << 2nVt$ or V_{in} varies in the range $[V_{ref} - 2nV_t: V_{ref} + 2nV_t]$, then the last equation can be rewritten as follows:

$I_{out} = \frac{I_b}{2nVt}\left(V_{in} - V_{ref}\right)$	Equation 6

The relation between I_{out} & I_b and the relation between I_{out} & V_{in} are linear. Equation 5 and Equation 6 can be combined into one equation as follows (Please note that in all next equations SI stands for Strong inversion and WI for stands for Weak inversion):

$I_{out} = \begin{cases} \sqrt{\frac{\beta_{5,4}}{n}}\sqrt{I_b}\left(V_{in} - V_{ref}\right) \rightarrow If V_{in} - V_{ref} << \sqrt{4nI_b/\beta_{5,4}} \;\&\; M4, M5 - SI \\ \frac{I_b}{2nVt}\left(V_{in} - V_{ref}\right) \rightarrow If V_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases}$	Equation 7

Equation 7 can be simplified as follows (Linear relation between I_{out} & I_b if M4 & M5 in Weak inversion, otherwise Square root relation in Strong Inversion):

$I_{out} = \begin{cases} a\sqrt{I_b} \rightarrow M4, M5 - SI \\ aI_b \rightarrow M4, M5 - WI \end{cases}$	Equation 8

where the parameter *a* can take positive and negative values and it is given by:

$$a = \begin{cases} \sqrt{\frac{\beta_{5,4}}{n}}\left(V_{in} - V_{ref}\right) \rightarrow If V_{in} - V_{ref} << \sqrt{4nI_b/\beta_{5,4}} \;\&\; M4, M5 - SI \\ \frac{\left(V_{in} - V_{ref}\right)}{2nVt} \rightarrow If V_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases}$$

To obtain the difference function, Equation 7 can also be simplified in the following way:

$I_{out} = b\left(V_{in} - V_{ref}\right)$	Equation 9

where the parameter *b* "it can take only positive values" is given by:

$$b = \begin{cases} \sqrt{\frac{\beta_{5,4}}{n}}\sqrt{I_b} \rightarrow If V_{in} - V_{ref} << \sqrt{4nI_b/\beta_{5,4}} \;\&\; M4, M5 - SI \\ \frac{I_b}{2nVt} \rightarrow If V_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases}$$

V_{in} can be the first variable input voltage (V_1) and V_{ref} the second variable input voltage (V_2). Then V_1-V_2 equals to the (I_{out}/b) value or I_{out} is proportional to V_1-V_2.

Equation 7 is voltage to current relation between I_{out} & V_{in} "the input is voltage and the output is current". It can also be seen as current to voltage, or voltage to voltage or current-to-current by adding Resistor "designed by Two CMOS transistors PMOS and NMOS" to Figure 4 as follows (see Table 1): resistor R_1 between V_{in} & V_{ref} to convert the input voltage to input current; and Resistor R_2 between I_{out} and V_{ref} to convert the output current to output voltage (see Figure 5). The value of R_1 and R_2 are controlled by the V_{n1}, V_{p1} , V_{n2} and V_{p2}. It is important to note that the circuit in Figure 5 will be connected to another circuit in Artificial Neural Network, in view of the fact that the output voltage I_{out}*R_1 of Figure 5 must be go as input to the gate of CMOS transistor of the circuit connected to Figure 5 to be sure that I_{out} will flow only in R_2.

TABLE 1

Voltage To Current "Figure 4"	$I_{out} = f(V_{in} - V_{ref})$
Current To Voltage "Figure 5"	$I_{out} \times R_1 = f\left(V_{in} - V_{ref} / R_2\right)$
Voltage To Voltage "Figure 5 without R_1"	$I_{out} \times R_1 = f(V_{in} - V_{ref})$
Current To Current "Figure 5 without R_2"	$I_{out} = f\left(V_{in} - V_{ref} / R_2\right)$

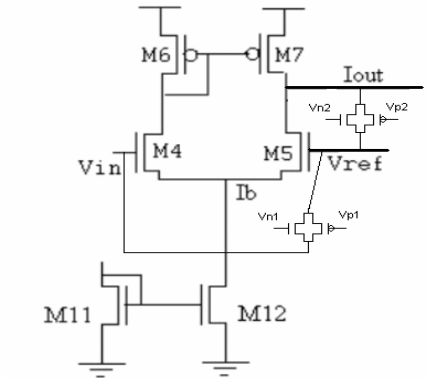

Figure 5. Figure 4 with input current and output voltage.

PARAMETRIC WIDE-SMALL RANGE LINEAR AND PARAMETRIC WIDE QUADRATIC RELATIONS

If the circuit in Figure 2 is combined with the circuit in Figure 4, then the circuit in Figure 6 is obtained.

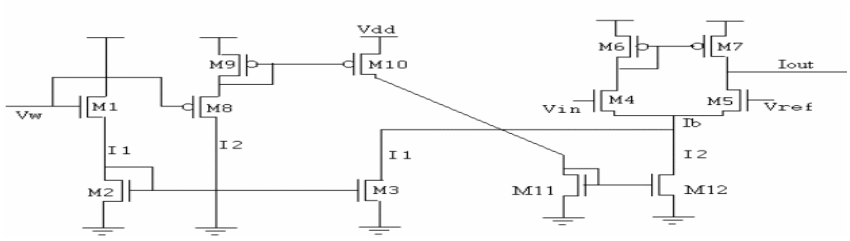

Figure 6. The circuit in Figure 2 + the circuit in Figure 4.

Consequently, Equation 3 is substituted in Equation 7 as in the following equation:

$$I_{out} = \begin{cases} \sqrt{\frac{\beta_{5,4}\beta_0}{2n^2}}|V_w - V_0|(V_{in} - V_{ref}) \rightarrow If V_{in} - V_{ref} << \sqrt{4nI_b/\beta_{5,4}} \;\&\; M4, M5 - SI \\ \frac{\beta_0}{4n^2 Vt}(V_w - V_0)^2(V_{in} - V_{ref}) \rightarrow If V_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases}$$

Equation 10

Where

1) V_w varies in the range [0: V_{dd}];
2) V_{in} varies in the range [V_{ref} - $\sqrt{4nI_b/\beta_{5,4}}$: V_{ref} + $\sqrt{4nI_b/\beta_{5,4}}$] if M4 and M5 work in strong inversion;
3) V_{in} varies in the range [V_{ref} -2nVt: V_{ref} +2nVt] if M4, M5 work in weak inversion.

It is clear that V_w range is wide [0:V_{dd}], while V_{in} range is smaller then V_w and its value depends on the M4 & M5 inversion region. Note that, if M4 and M5 work in strong inversion in Figure 6, the quadratic relation in Equation 3 substituted in the square root relation in Equation 7 becomes linear. Equation 10 can be seen as two-quadrant multiplier with respect to V_{in} and not V_w. It can be viewed in two modes:

Mode1:

$$I_{out} = \begin{cases} a_1|V_w - V_0| \rightarrow M4, M5 - SI \\ a_1(V_w - V_0)^2 \rightarrow M4, M5 - WI \end{cases}$$

Equation 11

where the parameter a_1 that can take positive and negative values, it is given:

$$a_1 = \begin{cases} \sqrt{\frac{\beta_{5,4}\beta_0}{2n^2}}\left(V_{in} - V_{ref}\right) \rightarrow If V_{in} - V_{ref} << \sqrt{4nI_b/\beta_{5,4}} \;\&\; M4, M5 - SI \\ \frac{\beta_0}{4n^2 Vt}\left(V_{in} - V_{ref}\right) \rightarrow If V_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases}$$

Note that: (1) The above equation gives us a wide range linear relation between I_{out} and V_w. While in Figure 4 & Equation 7 the range between I_{out} and V_{in} is limited. (2)It also gives us a wide range quadratic relation between I_{out} and V_w. (3)The relation between I_{out} and V_w is not static but is controlled by a parameter a1, which depends on the input V_{in}, while in Figure 2 and Equation 3 the quadratic relation is static and in Figure 4 & Equation 7 the linear relation between I_{out} and V_{in} is static as well.

Mode2:

$I_{out} = b_1\left(V_{in} - V_{ref}\right)$	Equation 12

where the parameter b_1 that can take only positive values, and it is given:

$$b_1 = \begin{cases} \sqrt{\frac{\beta_{5,4}\beta_0}{2n^2}}\left|V_w - V_0\right| \rightarrow M4, M5 - SI \\ \frac{\beta_0}{4n^2 Vt}\left(V_w - V_0\right)^2 \rightarrow M4, M5 - WI \end{cases}$$

Note that: (1) The range of V_{in} is limited "not as wide as V_w" and depends on M4 & M5 inversion region. (2) The Equation 12 is similar to Equation 9. However, here it is controlled by a parameter b_1 that depends on V_w and not by the parameter b, which depends on I_b. (3) The linear relation in the Equation 12 can be considered dynamic, while that of Equation 9 is static. (4) Equation 12 can be considered as a two quadrants multiplier with b_1 as a parameter that has always the same sign.

WIDE RANGE "LINEAR & QUADRATIC" MULTIPLIER

From the previous section the following results can be obtained: (1) Equation 12 & Figure 6 can be seen as a linear two-quadrant multiplier & the linear range of the multiplier depends on M4, M5 if they are working in strong or in weak inversion; (2) Equation 11 cannot be seen as two quadrants multiplier. It can be seen as one-quadrant only (if $a_1 > 0$ or $V_{in} > V_{ref}$" and $V_w > V_0$).

Now to make Four Quadrant multiplier, the following three steps must be done: (1) Add another OTA (M13, M14, M15, M16) to the circuit in Figure 6 as shown in Figure 7; (2) Take the output as the sum of I_{out1} and I_{out2}; (3) V_{in} must be connected to the gates of M4 and M14 and V_{ref} to M5 and M13. Because if V_{ref} in M14 and V_{in} in M13, I_{out1} and I_{out2} will have the same sign and then the multiplier will remain two-quadrant as in Figure 6. This mul-

tiplier can be viewed as a new version of the multiplier presented in (Chiblè, 2000; 2003a; 2003b), which take M13 & M14 as PMOS connected directly to M10, M15 & M16 as NMOS, and eliminate M11, M12.

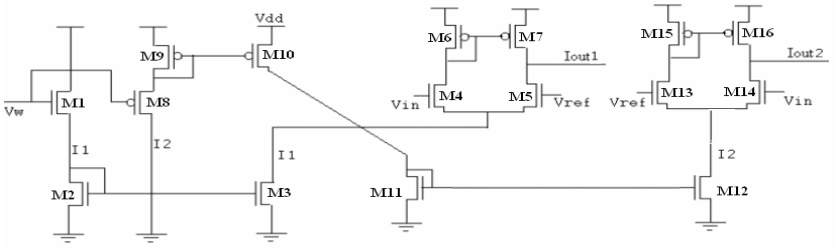

Figure 7. Four-quadrant multiplier.

Then the output current (I_{out} = I_{out1+} I_{out2}) of the four-quadrant multiplier is given by:

$$I_{out} = \begin{cases} I_{out1} \rightarrow V_w > V_o \\ I_{out2} \rightarrow V_w < V_o \end{cases}$$

where I_{out1} & I_{out2} are similar to Equation 10", then the above equation is given by:

$$I_{out} = \begin{cases} I_{out1} = \begin{cases} \sqrt{\frac{\beta_{5,4}\beta_0}{2n^2}}|V_w - V_0|(V_{in} - V_{ref}) \rightarrow IfV_{in} - V_{ref} << \sqrt{4nI_b/\beta_{5,4}} \;\&\; M4, M5 - SI \\ \frac{\beta_0}{4n^2Vt}(V_w - V_0)^2(V_{in} - V_{ref}) \rightarrow IfV_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases} \rightarrow V_w > V_o \\ I_{out2} = \begin{cases} \sqrt{\frac{\beta_{13,14}\beta_0}{2n^2}}|V_w - V_0|(V_{ref} - V_{in}) \rightarrow IfV_{in} - V_{ref} << \sqrt{4nI_b/\beta_{13,14}} \;\&\; M4, M5 - SI \\ \frac{\beta_0}{4n^2Vt}(V_w - V_0)^2(V_{ref} - V_{in}) \rightarrow IfV_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases} \rightarrow V_w < V_o \end{cases}$$

Assume "by designing" that $\beta_1 = \beta_{5,4} = \beta_{13,14}$, then I_{out} becomes as follows:

$I_{out} = \begin{cases} \sqrt{\frac{\beta_1\beta_0}{2n^2}}(V_w - V_0)(V_{in} - V_{ref}) \rightarrow IfV_{in} - V_{ref} << \sqrt{4nI_b/\beta_{5,4}} \;\&\; M4, M5 - SI \\ \frac{\beta_0}{4n^2Vt}(V_w - V_0)^2(V_{in} - V_{ref}) \rightarrow IfV_{in} - V_{ref} << 2nV_t \;\&\; M4, M5 - WI \end{cases}$	Equation 13

Explanation of all previous equations are summarized in TABLE 2.

SIMULATION RESULTS

The circuit has been designed and simulated by using WinSpice "wspice3 simulator for Windows" and by using the Parameters of the technology AMIS CMOS 0.35um and by using all models (typical, fast, slow), which is used for analog implementation. The dimensions "width and the length" of the MOS transistors have been computed on the base of the technology parameters (*e.g.* the mobility of the electron, oxide capacitor, *etc.*). Also, the dimensions of the transistors are calculated and designed based on the following considerations: 1) M1,M2,M3 are designed in a way to create I_1 with Von approximately equal to V_{ref}; 2)

M8,M9,M10,M11,M12 are designed in a way to create I_2 with Vop approximately equal to V_{ref}; 3) M4, M5, M13, M14 are designed in a way to make OTA work in weak inversion or in strong inversion; 4) M6, M7, M15, M16 are designed as current mirror. The dimensions are as follows: M1=1/1 - M2=4/8 - M3=1/8 - M6=4/4 - M7=4/4 - M8=1/1 - M9=4/8 - M10=4/8 - M11=4/8 - M12=4/8 - M15=4/4 -M16=4/4 – (weak inversion M4=25/2-M5=25/2-M13=25/2-M14=25/2) – (strong inversion M4=1/3-M5=1/3-M13=1/3-M14=1/3). The Maximum Power dissipation "MPD" of the circuit is given by multiplying the number of branches times the maximum current in the branch times the power supply voltage.

TABLE 2

Explanation of All Equations in This Paper

Number	Relation Type
Equation 1	Static Quadratic relation between output current and input voltage that varies in the range "V0 < Vw < Vdd".
Equation 2	Static Quadratic relation between output current and input voltage that varies in the range "0 < Vw < V0.
Equation 3	"Equation 1+Equation 2" Static Quadratic relation between output current and input voltage that varies in the range "0 < Vw < Vdd".
Equation 4	"Equation 1-Equation 2" Static Quadratic relation with 0< Vw < Vdd with positive and negative output current (It has positive and negative values).
Equation 5	Static Square Root Relation with respect to I_b which varies between 0 and $I_{b\text{-}max}$.
Equation 6	Static Linear Relation with respect to I_b which varies between 0 and I_{bmax}.
Equation 7	"Equation 5+Equation 6" Static general equation in strong and weak inversion
Equation 8	It is a linear relation "Strong Inversion" or Square root relation "Weak inversion"- Static relation
Equation 9	Static difference linear relation
Equation 10	Two quadrant multiplier that multiply V_{in} by V_w where V_{in} can be positive or negative and V_w is only positive. It can be viewed in two modes "as in Equation 11 and Equation 12".
Equation 11	Wide range linear "Strong Inversion" relation & Wide Range Quadratic relation "Weak inversion". It is a Dynamic relation where the parameter a_1 (which depends on V_{in}) controls the linear or quadratic relation "While note that Equations 1,2,3,4 are Static and not Dynamic"
Equation 12	Linear relation "in Strong or Weak inversion", the wideness of the linear relation in strong inversion is larger than in weak inversion – it is dynamic relation where the parameter b_1 (which depends on V_w) controls the linear relation slope "While note that Equation 9 is Static and not Dynamic";
Equation 13	It can be considered four-quadrant multiplier, which multiplies V_{in} by V_w where V_{in} & V_w can be positive or negative.

In this circuit the number of branches equals to Five [(1) M1,M2 - (2) M8,M9 - (3) M10,M11 - (4) M3,M4,M5,M6,M7 - (5) M12,M13,M14,M15,M16]; the maximum current in branch equals to 6μa; and the power supply voltage equals to 3.3V. Then MPD = 5 * 6μA * 3.3V = 99μW. If we reduce the maximum current then we can reduce the maximum power

dissipation. For example if maximum current is 1ua then MPD=16.5µW. The simulation results are presented in this section as follows:

A) I_1 & I_2 versus V_w

Figure 8 (right Figure) shows the simulation of the circuit proposed in Figure 1 and Equation 1 "I_1 (micro ampere) versus V_w (Volt)" where V_w varies between 0V and 3.3V with step 0.2 and I_1 varies between 0ua and 6ua. Figure 8 (left Figure) shows the simulation of the circuit proposed in Figure 2 and Equation 2 "I_2 versus V_w" where V_w varies between 0V and 3.3V with step 0.2 and I2 varies between 0ua and 6ua".

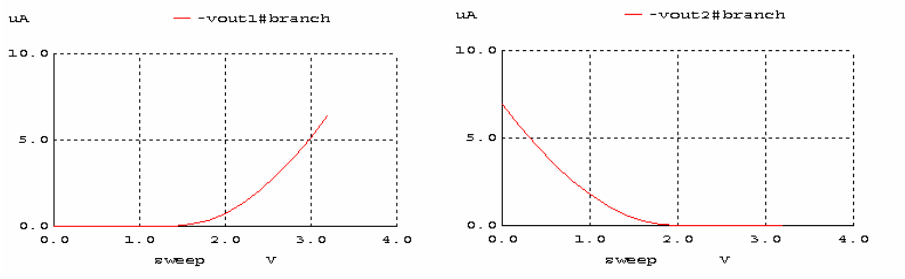

Figure 8. The simulation of the circuit proposed in Figure 1 & Equation 1 "I_1 versus V_w" (right Figure) and Figure 2 & Equation 2 "I_2 versus V_w" (left Figure).

B) I_b & I_{b2} versus V_w

Figure 9 (right Figure) shows the simulation of the circuit proposed in Figure 2 and Equation 3 "I_b versus V_w" where V_w varies between 0V and 3.3V with step 0.2 and I_b varies between 0ua and 6ua". Figure 9 (left Figure) shows the simulation of the circuit proposed in Figure 3 and Equation 4 "I_{b2} versus V_w" where V_w varies between 0V and 3.3V with step 0.2 and Ib2 varies between -6ua and 6ua".

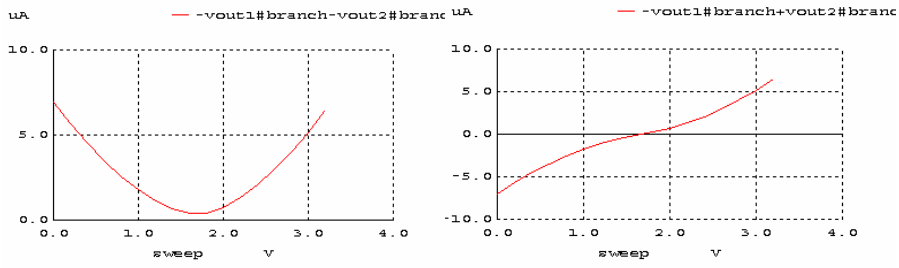

Figure 9. The simulation of the circuit proposed in Figure 2 and Equation 3 "I_b versus V_w" (right Figure) & in Figure 3 and Equation 4 "I_{b2} versus V_w" (left Figure).

C) I_{out} versus I_b

Figure 10 (right Figure) shows the simulation of the circuit proposed in Figure 4 and Equation 5 with M4 and M5 work in strong inversion; I_{out} versus I_b with V_{in} as a parameter that varies between 1.55V and 1.75V with step 0.05V while I_b varies between 0ua and 6ua with steps 0.1ua and Iout varies between -2ua and 2ua. Figure 10 (left Figure) shows the simulation of the circuit proposed in Figure 4 and Equation 6 with M4 and M5 work in weak inversion; I_{out} versus I_b with V_{in} as a parameter that varies between 1.55V and 1.75V with step 0.05V while I_b varies between 0ua and 6ua with steps 0.1ua and I_{out} varies between -5ua and 5ua.

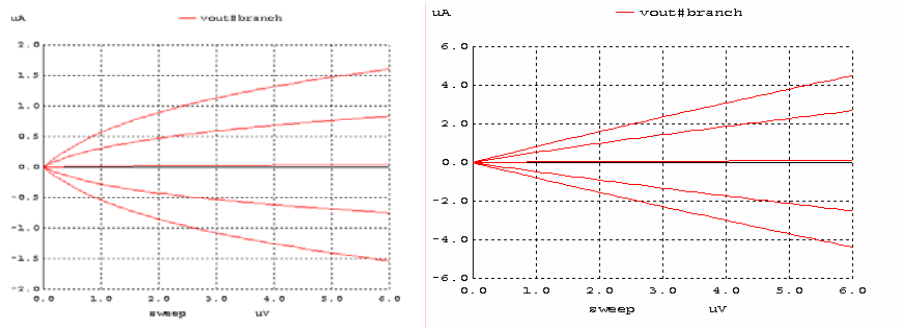

Figure 10. The simulation of the circuit proposed in Figure 4 "I_{out} versus I_b" & Equation 5 (right Figure) & Equation 6 (left Figure).

D) I_{out} versus V_{in}

Figure 11 shows the simulation of the circuit proposed in Figure 4 "I_{out} versus V_{in} where V_{in} varies between 0V and 3.3V with steps 0.2V while I_{out} varies in the range -6ua and 6ua". The right Figure is related to Equation 5 where the transistors M4 and M5 work in strong inversion and the left Figure is related to Equation 6 where the transistors M4 and M5 work in weak inversion. It is clear from Figure 4 that the linear range is more wide in strong inversion than in weak inversion.

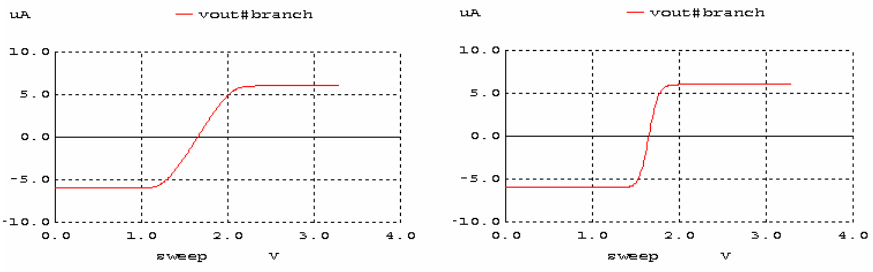

Figure 11. The simulation of the circuit proposed in Figure 4 "I_{out} versus V_{in}" & Equation 5 (right) & Equation 6 (left).

E) I_{out} versus V_w with parameter a_1

The Figure 12 (right) shows the simulation of the circuit proposed in Figure 6 and Equation 11 "I_{out} versus V_w with V_w varies between 0V and 3.3V with steps 0.2V and V_{in} as a parameter varies between 1.55V and 1.75V with steps 0.025V" where M4 and M5 work in weak inversion while in the (left) M4 and M5 work in strong inversion. The right figure gives a wide range quadratic relation while the left figure gives a wide range linear relation, which are controlled by the parameter a1 which is related to V_{in}.

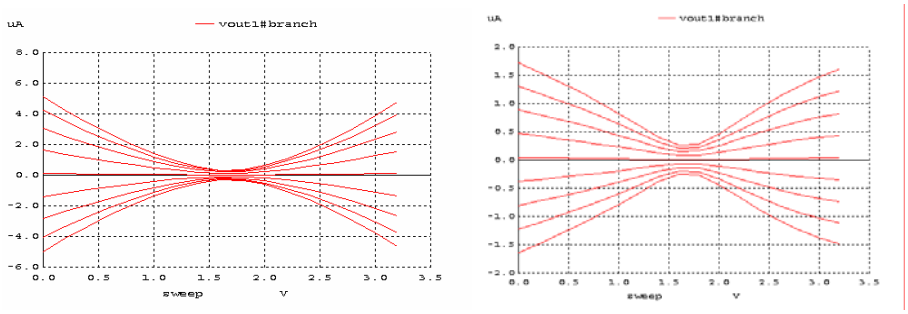

Figure 12. The simulation of the circuit proposed in Figure 6 & Equation 11 "I_{out} versus V_w" with M4 and M5 work in weak inversion (right) and with M4 and M5 work in strong inversion (left).

F) I_{out} versus V_{in} with parameter b_1

The Figure 13 (right) shows the simulation of the circuit proposed in Figure 6 and Equation 12 "I_{out} versus V_{in} with V_{in} varies between 1.45V and 1.85V with steps 0.1V and V_w as a parameter varies between 0V and 3.3V with steps 0.55V" with M4 and M5 that work in weak inversion while the (left) with M4 and M5 that work in strong inversion. The right and left Figures show Linear Relation in a special range, which controlled by the linear parameter b1 (right) and quadratic parameter b1 (left).

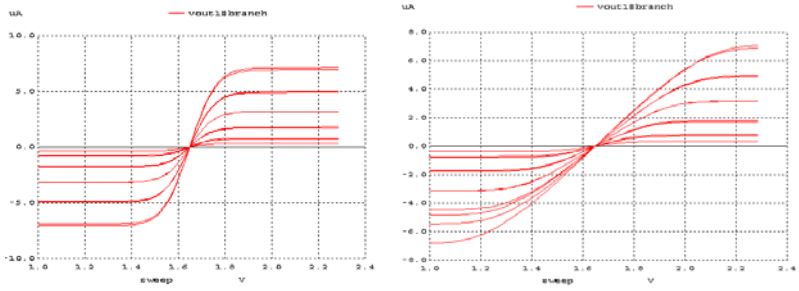

Figure 13. The simulation of the circuit proposed in Figure 6 & Equation 12 "I_{out} versus V_{in}" with M4 and M5 work in weak inversion (right) and with M4 and M5 work in strong inversion (left).

G) I_{out} versus V_w with paramter V_{in}

Figure 14 (right) shows the simulation of the circuit proposed in Figure 7 and Equation 13 with M4 and M5 work in Weak inversion "I_{out} [-5ua:+5ua] versus V_w [0V:3.3V] with parameter V_{in} that varies in the range [1.55V:1.75V] with step 0.01V". Figure 14 (Left) shows the simulation of the circuit proposed in Figure 7 and Equation 13 with M4 and M5 work in Strong inversion "I_{out} [-2ua:+2ua] versus V_w [0V:3.3V] with parameter V_{in} that varies in the range [1.55V:1.75V] with step 0.01V".

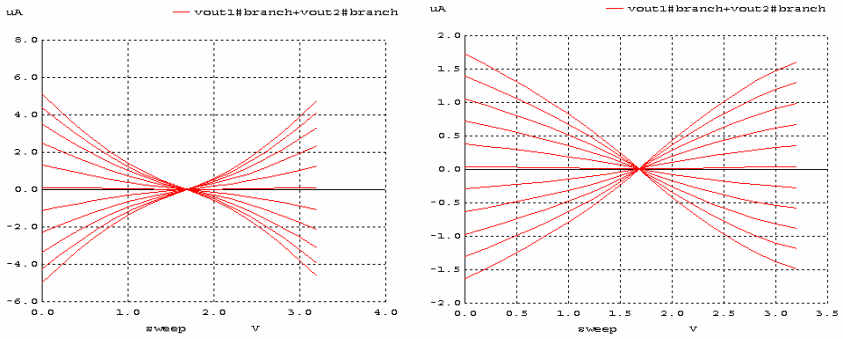

Figure 14. The simulation of the circuit proposed in Figure 7 and Equation 13 "I_{out} versus V_w" with M4 and M5 work in weak inversion (right) and with M4 and M5 work in strong inversion (left).

H) Iout versus Vin with parameter Vw.

Figure 15 (right) shows the simulation of the circuit proposed in Figure 7 and Equation 13 with M4 and M5 work in Weak inversion "I_{out} [-5ua:+5ua] versus V_{in} [1.55V:1.75V] with parameter V_w that varies in the range [0V:3.3V] with step 0.33V". Figure 15 (left) shows the simulation of the circuit proposed in Figure 7 and Equation 13 with M4 and M5 work in Strong inversion "I_{out} [-5ua:+5ua] versus V_{in} [1.25V:2.05V] with parameter V_w that varies in the range [0V:3.3V] with step 3.3V".

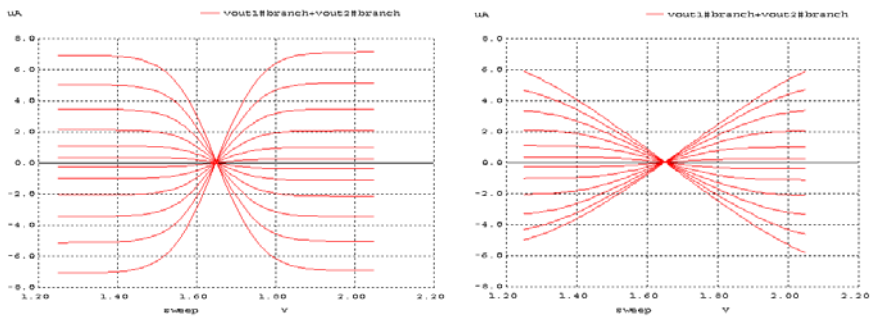

Figure 15. The simulation of the circuit proposed in Figure 7 and Equation 13 "I_{out} versus V_{in}" with M4 and M5 work in weak inversion (right) and with M4 and M5 work in strong inversion (left).

It is clear that from Figure 14 left and Figure 15 left, there is a good linear four quadrant multiplier with V_w that varies in the range [0V:3.3V] and V_{in} that varies in the range [1.25V:2.05V]. While from Figure 14 right and Figure 15 right, there is a non linear "quadratic relation" four quadrant with V_w that varies in the range [0V:3.3V] and V_{in} that varies in the range [1.55V:1.75V].

CONCLUSION

In the paper CMOS circuits were presented that implement different relations: Static & Dynamic Linear and Wide linear Relations; Static & Dynamic Wide Quadratic relations; Static Square Root Relations; Static & Dynamic difference linear relations; Two quadrant multiplier; and Four-quadrant multiplier. These relations can be used in many applications in signal processing and neural networks. All of these circuits can be realized in small area and low power consumptions. Figure 4 & Equation 9 can be used in the neuron module to compute the error which is the difference between the neuron target and the neuron output which is based on the random initial weights. Figure 7 & Equation 13 can be used in the synapse module as the analog multiplier that multiply the input by the weight and also as the analog multiplier that multiply the backward error "which is transmitted from the neuron toward the synapse" by the weight. The future work will be focused on using these relations to implement the neuron and synapse module to design Artificially Neural Network for specific applications.

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REFERENCES

Annema, A.J. 1995. *Feed forward neural networks*. Kluwer Academic Publishers.

Bo, G.M., Caviglia, D.D., Chiblè, H. and Valle, M. 1999. A circuit architecture for on-chip learning. *Analog Integrated Circuits & Signals Processing*, 18:163-173.

Chiblè, H. 1997. *Analysis and design of analog microelectronic neural network architectures with on-chip supervised learning*. Doctoral Dissertation. University of Genoa, Genoa, Italy.

Chiblè, H. 2000. Four quadrant multiplier for analog VLSI neural networks. *Lebanese Science Journal*, 1(2): 51-62.

Chiblè, H. 2003a. Experimental results of an analog VLSI multiplier/transconductance circuit. *Lebanese Science Journal*, 4(2): 73-85.

Chiblè, H. 2003b. Experimental results of an analog VLSI multiplier /synapse/transconductance circuit. *International Journal of Modeling & Simulation (IASTED / ACTA Press)*, 24(4): 224-230.

Ghandour, A. and Chiblè, H. 2007. *Advanced electronic circuits for artificial neural network system.* Final Research Report, Lebanese University.

Han, G. and Sinencio, E.S. 1998. CMOS transconductance multipliers: A tutorial. *IEEE Trans. on Circuit and Systems: II. Analog and Digital Signal Processing*, 45(12): 1550-1563.

Mead, C.A. 1989. *Analog VLSI and neural systems.* Addison-Wesley, Reading.

Prodanov, V.I. and Green, M.M. 1997. Bipolar/CMOS (weak inversion) rail-to-rail constant-gm input stage. *Electronics Letters*, 33(5): 386-387.

Saxena, N. and Clark, J.J. 1994. A four quadrant CMOS analog multiplier for analog neural networks. *IEEE Journal of Solid State Circuits*, 29(6): 746-749.

Valle, M., Caviglia, D.D. and Bisio, G.M. 1996. An experimental analog VLSI neural network with on-chip back-propagation learning. *Analog Integrated Circuits and Signals Processing*, 9: 231-245.

Vittoz, E.A. 1994. Analog VLSI signal processing: why, where and how? *Journal of VLSI Signal Processing*, 8: 27-44.