SPICE SIMULATION OF NEURAL NETWORKS MULTI-LAYER PERCEPTRON FOUR-QUADRANT CMOS ANALOG MULTIPLIER OTANNO

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ABSTRACT

In this paper, the OTANNO version of four-quadrant CMOS analog multiplier circuit for artificial neural networks multi layer perceptron operation will be proposed. The proposed multiplier can be divided into two or three parts, which will be in the input, synapse and neuron. The percentage of silicon area saving is 95% with respect to that multiplier presented in (Chiblè, 1997). A comparison between OTANNO and OTANPS is also presented.

Keywords: neural networks, multi layer perceptron, on-chip & off-chip learning, multipliers, synapse, analog signal processing, CMOS circuit

INTRODUCTION

Neural networks multi layer perceptron have two basic modules: neuron and synapse. Each synapse needs a multiplier to multiply the weight by the input. Because the network or the fabricated chip can have hundreds or thousands of synapses, then the multiplier synapse circuit must have enough small silicon area and low power consumption. Neural networks are implemented in analog circuits and they are generally faster and require less hardware than digital VLSI implementations (Mead & Ismail, 1989; Vittoz, 1994).

Examples of artificial neural networks were presented (Hollis & Paulos, 1990; Han, 2007; Chiblè, 1997). MOS analog multipliers used to build an artificial neural networks were adopted in (Hollis & Paulos, 1990). A biologically inspired hardware implementation of neural networks with programmable conductance which was explained in (Han, 2007) presents an on-chip learning multi layer perceptron neural networks trained by the back propagation algorithm was designed in (Chiblè, 1997).

Examples of analog multipliers were presented (Naderi *et al*., 2007; Purushothaman, 2008; Sawigun & Mahattanakul, 2008; Chunhong & Zhengl, 2006; Zhangcai *et al*., 2006;

Sawigun & Demosthenous, 2006; Boonchu & Surakampontorn, 2005; Dastjerdi & Sarpeshkar, 2002; Sawigun *et al*., 2007; Singh & Radhakrishna, 2006; Kapanoglu & Yildirim, 2004; Lee *et al*., 1995; Saxen & Clark, 1994; Koosh & Goodman, 2001).

Valle *et al*. (1996) proposed a non-linear exponential relation multiplier to implement the synapse. Chiblè (1997) proposed a quadratic relation multiplier instead of an exponential relation to improve the neural networks learning. Chiblè (2000) proposed a linear relation multiplier instead of a quadratic relation to get the ideal case. The multiplier has been fabricated and successfully tested (Chiblè, 2004). Chiblè (2008) and Chiblè and Ghandour (2009) present two modified versions of the multiplier proposed in (Chiblè, 2000). In (Chiblè, 2008) OTANPS, the layout is simplified and the number of transistors of each synapse is decreased by four transistors. In (Chiblè & Ghandour, 2009) OTANN, the effect of electron mobility between P-channel and N-channel has been cancelled due to the use of the same type of transistors N-type or P-type differential pairs.

In this paper, the OTANNO version is proposed in order to simplify the layout and get less silicon area. The proposed multiplier was based on OTANN (Chiblè & Ghandour, 2009) but with one current mirror instead of two. Some of the simulation results were published in (Chiblè & Jouni, 2010). This paper includes the following sections: the proposed multiplier circuit; the simulations results (transistor dimensions - DC transfer characteristics - transient response - power consumption); multi layer perceptron synapse implementation, comparison with OTANPS version; use of the proposed multiplier OTANNO in previous fabricated chip; conclusion.

THE PROPOSED MULTIPLIER CIRCUIT

Preface

The proposed multiplier circuit is shown in Figure 1 and it is based on the multiplier presented previously (Chiblè, 2008; Chiblè & Ghandour, 2009). V_w is connected to the gates of M1 and M8. The circuit is designed in such a way that the currents I_1 & I_2 are flowing from V_{dd} to ground and one of them will flow at any time. The multiplier (Chiblè, 2008) was called OTANPS because it is composed of one N-channel OTA & One P-channel OTA & with Shortcut between I_1 and I_2. While the multiplier in (Chiblè & Ghandour, 2009) was called OTANN because it is composed of two N-channel OTA. The proposed multiplier is called OTANNO because it is composed of two N-channel OTA "OTANN" and only One current mirror (M15-6, M16-7) instead of two current mirrors (M15, M16 and M6, M7) (Chiblè & Ghandour, 2009). The proposed multiplier can be divided into two or three parts instead of being in a whole part:

The first part of the circuit can be embedded inside the input and it contains the following transistors (M1, M2, M3, M8, M9, M10, M11 and M12);

The second part of the circuit can be embedded inside the synapse and it contains the following transistors (M4, M5, M13 and M14);

The third part can be embedded inside the neuron and it contains the following transistors (M15-6, M16-7).

The proposed circuit as a whole part or two parts can be used for the implementation of multi layer perceptron neural network trained by the back propagation algorithm "on-chip learning" (Chiblè, 1997; Cairns & Tarassenko, 1995). As for the proposed circuit as a three parts,it can be used for the implementation of a feed forward neural networks "off-chip learning or chip in the loop learning" (Koosh & Goodman, 2001). In the case of three parts: the first part of the circuit must be embedded inside the input while the second part (the main part of multiplier) must be fixed in the synapse module, and the third part can be embedded inside the neuron. In the case of two parts, the first and second parts must be together.

The main advantage of three parts multiplier is to save the silicon area by reducing ten transistors in each analog multiplier (two in the neuron module and eight in the input) and consequently ten transistors in each synapse in the neural networks .Hence it will save ten transistors multiplied by the number of synapses. Another advantage is the no-presence of the effect of the electrons mobility due to the use of two N-channel differential-pair transistors instead of N-channel and P-channel (Chiblè, 2008).

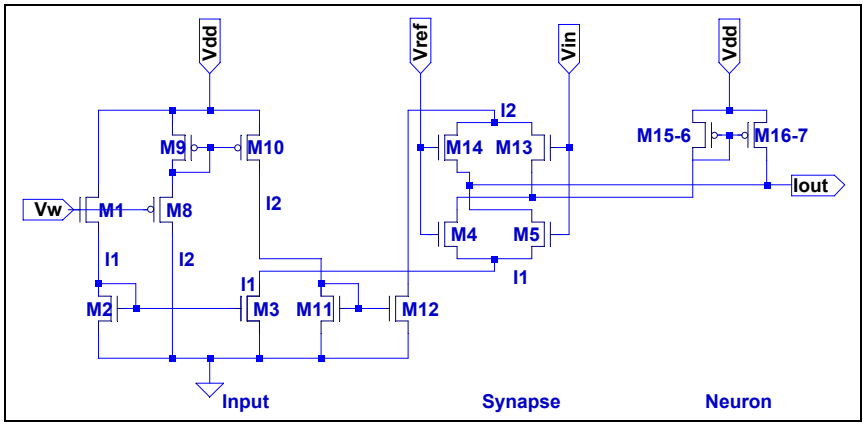

Figure 1. The multiplier circuit.

Multiplier equation

The output current of the multiplier I_{out} is given by:

$$I_{out} = \begin{cases} I_{out-n1} \xrightarrow{If} V_{ref} < V_w < V_{dd} \\ -I_{out-n2} \xrightarrow{If} 0 < V_w < V_{ref} \end{cases} \quad (1)$$

Where $I_{out\text{-}n1}$ & $I_{out\text{-}n2}$ are the output currents produced by the differential-pair M4 & M5 and M13 & M14 respectively. V_{dd} is the supply voltage and V_{ref} is the reference voltage ($V_{dd}/2$). If M4, M5, M13, M14 work in strong inversion, then $I_{out\text{-}n1}$ and $I_{out\text{-}n2}$ are given by (see Chiblè (2000) for their derivations):

$$I_{out-n1} = \sqrt{\frac{\beta_{4,5}}{n}}\sqrt{I_1}\left(V_{in} - V_{ref}\right) \qquad (2)$$

$$I_{out-n2} = \sqrt{\frac{\beta_{13,14}}{n}}\sqrt{I_2}\left(V_{ref} - V_{in}\right) \qquad (3)$$

Where $\beta_{4,5}$, $\beta_{13,14}$ are the transfer parameters of transistors M4/M5, M13/M14, and V_{in} varies in the range [1.55:1.75]. The currents I_1 and I_2 were calculated (Chiblè, 2000):

$$I_1 = \frac{\beta_n}{2n} \times \left(V_w - nV_{TH2} - V_{TH1}\right)^2 \qquad (4)$$

$$I_2 = \frac{\beta_p}{2n} \times \left(V_w - n^2 V_{dd} + nV_{TH9} + V_{TH8}\right)^2 \qquad (5)$$

Where n varies between 1 and 2 (Vittoz, 1994), V_{TH1}, V_{TH2}, V_{TH8} and V_{TH9} are the gate threshold voltages of M1, M2, M8 and M9 respectively, β_n and β_p are the transfer parameters of transistors M1, M2, M8 and M9 (Chiblè, 2000).

By well designing the transistors dimensions, the following approximations can be considered:

$$V_{ref} \approx nV_{TH2} + V_{TH1} \approx n^2 V_{dd} - nV_{TH9} - V_{TH8}$$

$$\beta_x \approx \frac{\beta_n}{2n} \approx \frac{\beta_p}{2n} \quad \& \quad \beta_y \approx \sqrt{\frac{\beta_{4,5}}{n}} \approx \sqrt{\frac{\beta_{13,14}}{n}}$$

By substituting the above approximations in equations (2), (3), (4), and (5), I_{out} becomes:

$$I_{out} = \begin{cases} \beta_y\sqrt{\beta_x}\left(V_w - V_{ref}\right)\left(V_{in} - V_{ref}\right) \xrightarrow{If} V_{ref} < V_w < V_{dd} \\ -\beta_y\sqrt{\beta_x}\left(V_w - V_{ref}\right)\left(V_{ref} - V_{in}\right) \xrightarrow{If} 0 < V_w < V_{ref} \end{cases}$$

Or

$$I_{out} = \beta_y\sqrt{\beta_x}\left(V_w - V_{ref}\right)\left(V_{in} - V_{ref}\right) \xrightarrow{If} 0 < V_w < V_{dd}$$

The last equation represents the multiplication of the multiplier circuit, where it is clearly the direct multiplication process between the two inputs V_{in} and V_w. Where V_{in} varies in the range [1.55V: 1.75V] and V_w varies in the range [0:V_{dd}] and V_{ref} is the reference ground voltage (1.65V) and V_{dd} is the supply voltage (3.3V).

SIMULATION RESULTS

The proposed circuit was designed and simulated by using the WinSpice "Wspice3 Simulator for Windows" and by using the spice level 8 and the parameters of a CMOS 0.35µm technology.

Multiplier transistor dimensions

The dimensions "width and the length" of the MOS transistors were computed based on the technology parameters (*e.g*. the mobility of the electron, oxide capacitor, *etc*…). The final designed dimensions were presented in details (Chiblè & Jouni, 2010). The dimensions were calculated and designed by taking the following considerations:

M1, M2, M3 are designed in a way to create $I_1 \approx 0$ when V_w is less than or equal to V_{ref};

M8, M9, M10 are designed in a way to create $I_2 \approx 0$ when V_w is greater than or equal to V_{ref};

M4, M5, M13, M14 are designed in a way to make the two N-channel differential-pair transistors work in strong inversion region;

The dimensions of the transistors M4, M5, M13, and M14 must be equal;

M15-6 and M16-7 are designed as current mirror.

The final designed dimensions (width µm/Length µm) of each transistor are the following: M1=1/1 - M2=4/8 – M3=1/8 – M4=3/3 – M5=3/3 – M8=1/1 – M9=4/8 – M10=4/8 - M11=1/8 - M12=1/8 - M13=3/3 - M14=3/3 - M15-6=4/4 – M16-7=4/4.

Multiplier dc transfer characteristics

The output current of the proposed multiplier I_{out} *versus* the input voltage V_w and the output current I_{out} *versus* the input voltage V_{in} are shown respectively in Figure 2 and Figure 3:

I_{out} in Figure 2 varies in the range [-2.5µA:2.5µA] and V_w varies in the range [0:3.3] with step 0.3 and with V_{in} as parameter varies in the range [1.55:1.75] with step 0.01.

I_{out} in Figure 3 varies in the range [-2.5µA:2.5µA] and V_{in} varies in the range [1.55:1.75] with step 0.01 and with V_w as parameter varies in the range [0:3.3] with step 0.3.

Multiplier transient response

To investigate the behaviour of the circuit as a modulator, the transient response of the synapse multiplier circuit must be established. The simulation result is shown in Figure 4 and Figure 5. Figure 4 shows the first input of sinusoidal voltage signal of 1MHz frequency and peak to peak voltage 3.3V and the second input of sinusoidal voltage of 10MHz frequency and peak to peak voltage 100mV. Figure 5 shows the multiplier output which is the modulated signal.

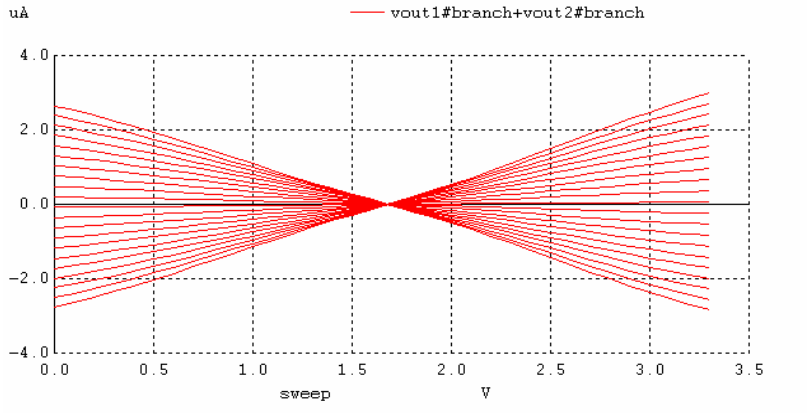

Figure 2. I_{out} *versus* V_w and with V_{in} as a parameter.

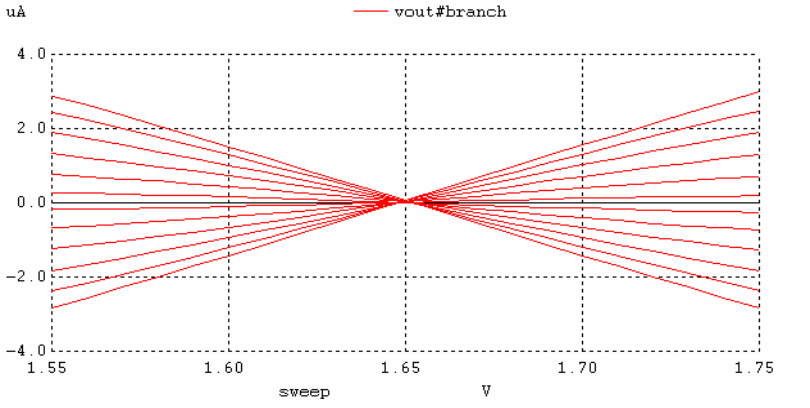

Figure 3. I_{out} *versus* V_{in} and with V_w as a parameter.

Multiplier power consumption

The circuit consumption is measured by the maximum power consumption "MP" of the circuit, which is given by multiplying the power supply voltage V_{dd} times the sum of the

maximum current that flows in the multiplier circuit. The proposed circuit has five branches (M1, M9, M10, M15-6, and M16-7). If M4 & M5 are on or work (V_w>V_{ref}) then M13 & M14 are off and *vice versa* if (V_w<V_{ref}), then MP is given by:

$$MP = \begin{cases} \text{MP (M1)} + \text{MP (M15 - 6)} + \text{MP (M16 - 7)} & \xrightarrow{\text{if}} V_w > V_{ref} \\ \text{MP (M8)} + \text{MP (M10)} + \text{MP (M15 - 6)} + \text{MP (M16 - 7)} & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

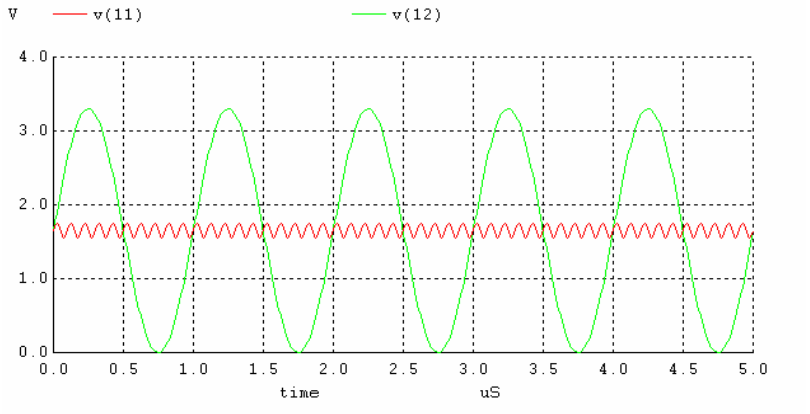

Figure 4. The multiplier two input sinusoidal voltages V_{in} and V_w.

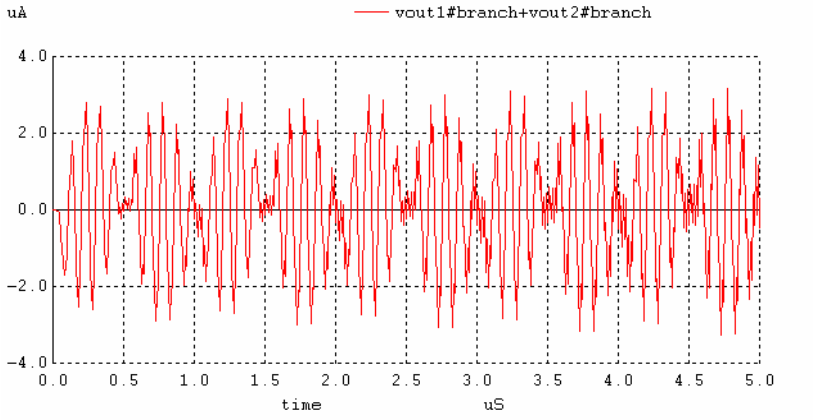

Figure 5. The multiplier output signal I_{out}.

where MP(M1) is the maximum power consumption in M1 branch that also contains M2, and it is given by the multiplication of the maximum current $I_{max(M1)}$ that flows in M1 branch times the V_{dd}:

$$\text{MP (M1)} = \text{Imax(M1)}*\text{Vdd}$$

The same for other branches:

$$MP\ (M15\text{-}6) = I_{max(M15\text{-}6)} * V_{dd}$$
$$MP\ (M16\text{-}7) = I_{max(M16\text{-}7)} * V_{dd}$$
$$MP\ (M8) = I_{max(M8)} * V_{dd}$$
$$MP\ (M10) = I_{max(M10)} * V_{dd}$$

Then MP becomes:

$$MP = V_{dd} \begin{cases} I_{max(M1)} + I_{max(M15\text{-}6)} + I_{max(M16\text{-}7)} & \xrightarrow{\text{if}} V_w > V_{ref} \\ I_{max(M8)} + I_{max(M10)} + I_{max(M15\text{-}6)} + I_{max(M16\text{-}7)} & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

The differential pair "M4 & M5" equations are given by:

$$\begin{cases} I_{out} = I_4 - I_5 \\ I_1 = I_4 + I_5 \end{cases} \xrightarrow{then} I_{out} + I_1 = 2 * I_4 \xrightarrow{then} I_4 = \frac{I_{out} + I_1}{2}$$

Where I_4 and I_5 are the drain source currents in M4 and M5. From the current mirror concept, one has:

$$I_1 = I_{max(M1)}$$
$$I_2 = I_{max(M8)} = I_{max(M10)}$$
$$I_4 = I_{max(M15\text{-}6)} = I_{max(M16\text{-}7)}$$

By designing well the dimensions of transistors, one gets:

$$I_{max(M1)} = I_{max(M8)} = I_{max(M10)}$$

MP becomes:

$$MP = V_{dd} \begin{cases} 2 * I_{max(M1)} + I_{out} & \xrightarrow{\text{if}} V_w > V_{ref} \\ 3 * I_{max(M8)} + I_{out} & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

From the simulation results, V_{dd}=3.3V, $I_{max(M1)}$ = 6μA and I_{out} = 2.5μA, then:

$$MP = 3.3V \begin{cases} 2 * 6\mu A + 2.5\mu A \\ 3 * 6\mu A + 2.5\mu A \end{cases} = \begin{cases} 47.85\mu W & \xrightarrow{\text{if}} V_w > V_{ref} \\ 67.65\mu W & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

Finally the MP of the multiplier circuit as a whole part is 67.65μW (worst case). The power in the case of three parts multiplier will be consumed in the input and the neuron module and not inside the synapse module which will dissipate power (drain source voltage * drain source current). The input will consume 39.6μW because:

$$MP = V_{dd} \begin{cases} I_{max(M1)} \\ I_{max(M8)} + I_{max(M10)} \end{cases} = \begin{cases} 19.8\mu W & \xrightarrow{\text{if}} V_w > V_{ref} \\ 39.6\mu W & \xrightarrow{\text{if}} V_w < V_{ref} \end{cases}$$

The neuron will consume 28.05μW:

$$MP = V_{dd}\left(I_{max(M15\text{-}6)} + I_{max(M16\text{-}7)}\right) = V_{dd}\left(I_{out} + I_{max(M1)}\right) = 28.05\mu W$$

MULTI LAYER PERCEPTRON SYNAPSE IMPLEMENTATION

This section will explain the implementation of the proposed multiplier circuit in the multi layer perceptron neural networks.

Figure 1 can be viewed as in Figure 6. The input part contains 8 transistors, while the synapse part contains 4 transistors and the neuron part contains 2 transistors. They are connected together through metal wires. Figure 7 shows a black boxes model of the multiplier presented in Figure 6.

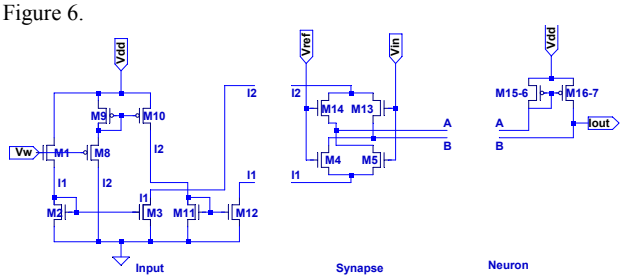

Figure 6. The three parts of the multiplier.

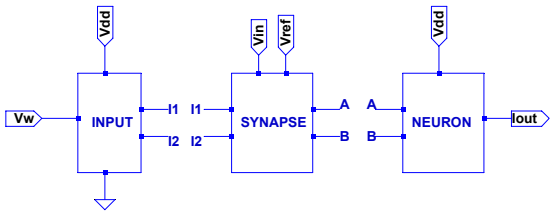

Figure 7. The multiplier as three black boxes.

Figure 8 shows one layer of a Multi Layer Perceptron artificial neural network where the inputs to synapses are "V_{in1}, V_{in2}, ….., V_{inN}" and the outputs of neurons blocks are "I_{out1}, I_{out2}, ….., I_{outM} ". The neuron block in Figure 8 indicates only the part of the proposed multiplier, while the neuron must contain a non linear function. If the layer is the first layer, then the number of inputs equals to the number of inputs that represents the pattern to be learned, while the number of neurons in each layer equals to the number of hidden neurons. If the layer is the last layer, then the number of inputs equals to the number of hidden neurons, while the number of output represents the number of output neurons which represents the classification and the results. The number of synapses equals the multiplication of inputs times outputs "N*M". Each synapse needs a multiplier to multiply the input while is the voltage times the weight and produces an output as current. For example, the synapse NM multiplies the weight V_{wNM} times the input V_{inN} and produces a fraction of the output $I_{outM,}$ knowing that the I_{outM} equals the sum of synapses in row M. As a conclusion, the neural networks system may contain thousands of multipliers; because of that, the area and the power consumption must be as small as possible.

The simulation of one synapse connected to one neuron as in Figure 7 (I_{out} *versus* V_w) is shown in Figure 10 and the simulation of ten synapses connected to one neuron as in Figure 9 (I_{out} *versus* V_w) is shown in Figure 11. It is clear that the values in Figure 11 equal the values in Figure 10 times the number of synapses "10". This will verify the correct operation of the proposed multiplier.

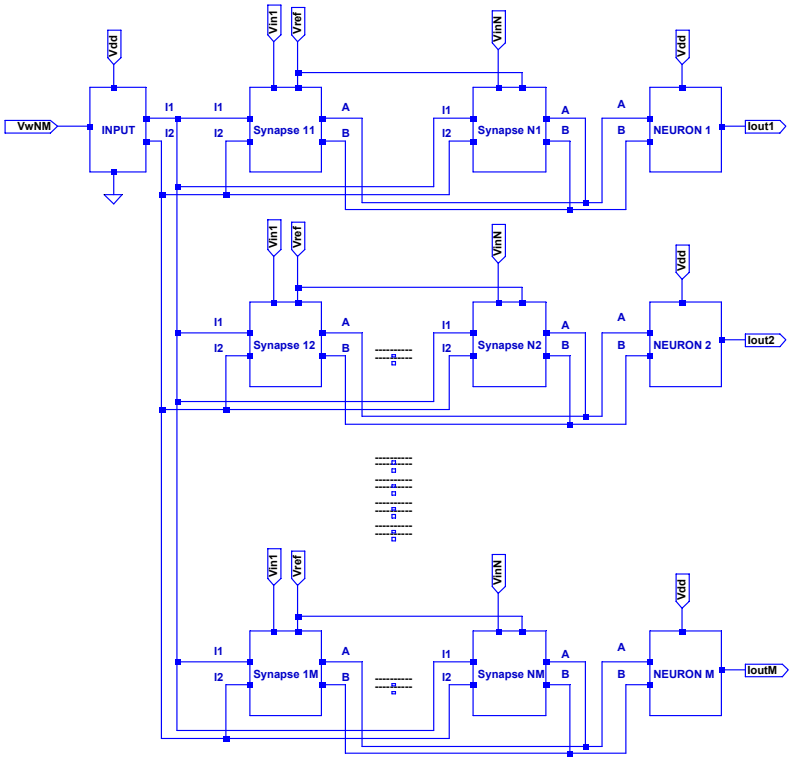

Figure 8. One layer of multi layer perceptron.

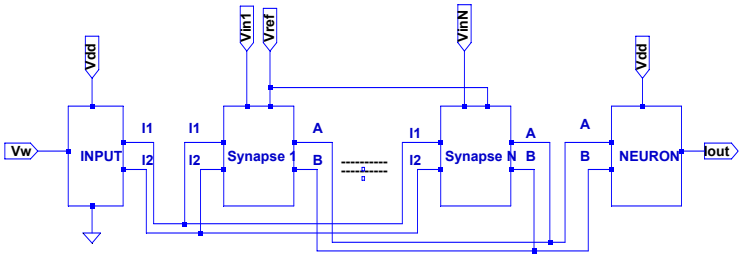

Figure 9. N synapses connected to one neuron.

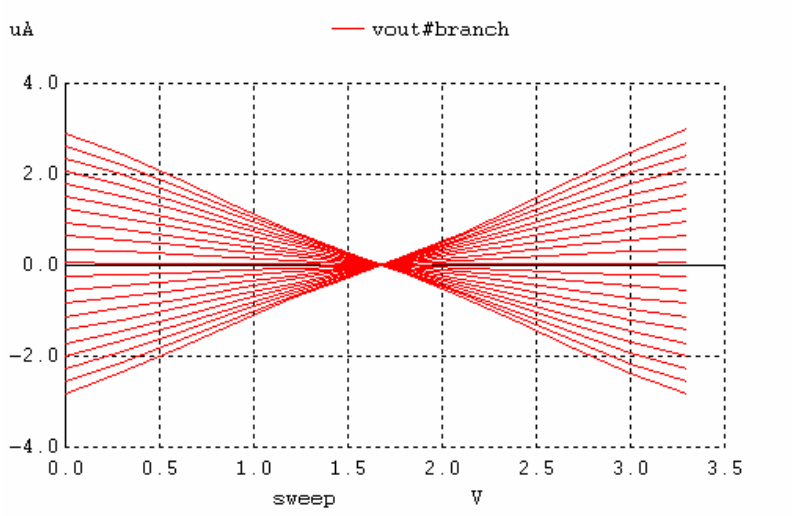

Figure 10. I_{out} *versus* V_w and with V_{in} as a parameter (one synapse connected to one neuron).

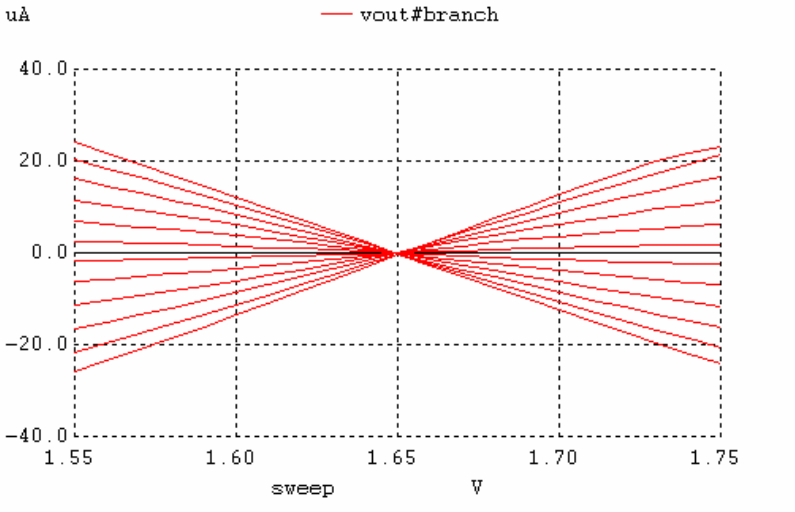

Figure 11. I_{out} *versus* V_w and with V_{in} as a parameter (ten synapses connected to one neuron).

COMPARISON WITH OTANPS VERSION

Comparison between the proposed multiplier version and other previous multiplier (Chiblè, 1997; 2000; 2004; 2008; Chiblè & Ghandour, 2009) versions is explained and presented in details (Chiblè & Jouni, 2010). Table 1 shows especially the comparison between the proposed multiplier OTANNO and the published OTANPS (Chiblè, 2008):

TABLE 1

Comparison between the Proposed Multiplier OTANNO and the OTANPS

	OTANPS (Chiblè, 2008)	This multiplier (OTANNO)
Neuron Module	4 transistors	2 transistors
Synapse Module	10 transistors	4 transistors
Input Module	No transistors	8 transistors
Total	14 transistors	14 transistors
Electron Mobility Effect	Yes	No
Layout design	More complex	Less Complex
Same Multiplier Equation	$I_{out} = \beta_y \sqrt{\beta_x}\left(V_w - V_{ref}\right)\left(V_{in} - V_{ref}\right) \xrightarrow{If} 0 < V_w < V_{dd}$	
Weight Bias current	One current $I_{12} = \begin{cases} \beta_x \times \left(V_w - V_{ref}\right)^2 \xrightarrow{if} V_{ref} < V_w < V_{dd} \\ -\beta_x \times \left(V_w - V_{ref}\right)^2 \xrightarrow{if} 0 < V_w < V_{ref} \end{cases}$	Two currents $I_1 = \frac{\beta_n}{2n} \times \left(V_w - nV_{TH2} - V_{TH1}\right)^2$ $I_2 = \frac{\beta_n}{2n} \times \left(V_w - n^2 V_{dd} + nV_{TH9} + V_{TH8}\right)^2$
DC characteristics for 1 synapse	Same results	Same results
DC characteristics for more synapses	Results obtained for 5 synapses connected to one neuron	Results obtained for 10 synapses connected to one neuron
Transient response analysis	No results obtained	Good results obtained

USING THE PROPOSED MULTIPLIER IN PREVIOUS FABRICATED CHIP

The Ph.D. thesis in (Chiblè, 1997) presents a fabricated chip multi layer perceptron neural network trained by the back propagation algorithm, where the multiplier is the basic element in the synapse module. The chip is on-chip learning, and then the multiplier with two parts will be taken for comparison. The network has 8 inputs and 16 hidden neurons and 4 output neurons. This means, it has 192 synapses (8*16+16*4) and 20 neurons (16+4). This section shows the results by using the proposed multiplier instead of that used for fabrication in (Chiblè, 1997).

Table 2 and Table 3 show the results of using Figure 1 as a whole part multiplier and Figure 6 (first part = input + synapse and second part = neuron) as two parts multiplier.

The percentage of silicon area saving "if one uses the two parts instead of a whole part" is 23% and the percentage of power consumption saving is 11%.

TABLE 2

The Silicon Area Reduction of Using the Two Parts Proposed Multiplier instead of One Part Multiplier

Silicon area	Area of one synapse μm^2	Numbers according to Chiblè (1997)	Area will be according to Chiblè (1997) μm^2
Figure 1 (whole part)	400	192	400*192=76000
Figure 6 (synapse)	300	192	300*192=57600
Figure 6 (neuron)	60	20	60*20=1200
The total area will be		=57600+1200=58800 μm^2	
The percentage silicon area saving		=1-57600/76000=23%	

TABLE 3

The Power Consumption Reduction of Using the Two Parts Proposed Multiplier instead of One Part Multiplier

Power Consumption	Power Consumption of one synapse	Power Consumption will be according to Chiblè (1997)
Figure 1 (whole part)	47.85µW	9187.2 µW
Figure 6 (synapse)	39.6 µW	7603.2 µW
Figure 6 (neuron)	28.05 µW	561 µW
Total Power Consumption will be		8164.2 µW
The percentage Power Consumption saving		11%

Table 4 shows a comparison between the proposed multiplier and the real dimensions presented in the fabricated chip (Chiblè, 1997). The silicon area of each multiplier circuit will be reduced from $6059\mu m^2$ to $300\mu m^2$ (silicon area saving is 95.048%). Then the area of hidden synapse module will be decreased by 30.47%, and the area of output synapse module will be decreased by 24.2%, while the hidden neurons and output neurons increase by 0.35% and 0.26% respectively (very small effect on silicon size). The new total silicon area is reduced by 25.7%.

CONCLUSION

In this paper, the OTANNO version of four-quadrant analog multiplier is presented. The multiplier can be used especially in neural networks applications and also in other signal processing operations. The multiplier circuit can be divided into two or three parts. Consequently, the synapse silicon area and the power dissipation will be decreased. The simulation results are presented; some of the related simulations of the proposed multiplier can be found in (Chiblè & Jouni, 2010). A comparison between the proposed multiplier and other multipli-

ers is also presented. The saving of multiplier silicon area is 95% between the proposed multiplier and that one presented in (Chiblè, 1997). As a result, the chip silicon area saving is 26%. The future work will be based on building a neural network with feed forward and backward operations.

TABLE 4

Neurons and Synapses Silicon Area Reduction by Using the Proposed Multiplier

	Silicon Area (Chiblè, 1997) μm^2	New Silicon Area μm^2	Number used (Chiblè, 1997)	Total Silicon Area (Chiblè, 1997) μm^2	New Total silicon area μm^2	Percentage saving area
Hidden synapse	140*135 =18900	=18900+300 -6059 =13141	128	2419200	1682048	30.47%
Output synapse	170*140 =23800	=23800+300 -6059 18041	64	1523200	1154624	24.20%
Hidden Neuron	155*110 =17050	=17050+60 17110	16	272800	273760	-0.35%
Output Neuron	168*140 =23520	=23520+60 23580	4	94080	94320	-0.26%
The total silicon area				4309280	3204752	25.63%

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