A PROGRAMMABLE RESOLUTION A/D CONVERTER MODELING

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(Received 1 December 2005 - Accepted 29 April 2006)

ABSTRACT

This paper describes a VHDL implementation of a behavioural model for novel programmable resolution analog to digital converters (ADCs). This architecture uses the dichotomic method in the conversion. The goal for using this VHDL description is to validate the algorithm conversion and facilitate the synthesis of the digital part. In this example it includes digital control of dichotomic method. The structure of the converter is composed of a reference voltage generator, a programmable gain amplifier and a low resolution ADC. An ADC of 12-bits has been modeled and simulated using VHDL. The Static Test Ramp Method is applied for the testing of the 12bits ADC models. Also, we show how the analog parts affect the linearity of ADC. Static parameters such as INL and DNL are determined and presented.

Keywords: A/D converter, programmable gain amplifier, modeling, test ramp, VHDL

INTRODUCTION

The analog-to-digital converter (ADC) is a key building block in digital communication receivers employing digital signal processing techniques. In bridging the analog and digital domains, the performance of the ADC often limits the achievable performance of the receiver. Many architectural choices in a receiver are affected by the A/D converter architecture. The key parameters which generally characterize A/D converter architectures are speed, resolution, and power. In a wide variety of CMOS analog circuits such as switched-capacitor filters (Amourah *et al*., 2002), algorithmic A/D convertors (Blecker *et al*., 2000), sigma-delta convertors (Aboushady *et al*., 2002; Chen *et al*., 2003; Rizzi & Castagnolo, 2006), sample-and-hold amplifiers, and pipeline A/D convertors (Min *et al*., 2003; Yoo *et al*., 2003; Parenti *et al*., 2005), speed and accuracy are determined by the settling behavior of the operational amplifier.

The use of behavioral models helps in achieving the target. Behavioral simulators work much faster than the transistor level counterparts thus permitting to explore all the regions of operation. Moreover, designer can use the electrical design features (like the gain, the bandwidth, the offset, the parasitic elements and so forth) as parameters of the behavioral model. Therefore, the behavioral simulation allows the designer to estimate the effect of basic blocks limitations on the converter performances. Also, the specifications of the data converter permit to extract the electrical specifications of the building blocks (Maloberti *et al.*, 1997).

The analog hardware description languages have received an increasing interest over the last years. The development of analog models suitable for VHDL description is a challenging issue (Rosinski & Vachoux, 1998; Vachoux *et al*., 1997; Acosta *et al*., 1999). Evidently, the implementation of an analog behavioral model that is deeply related to the logical description of a digital system is possible in mixed-mode simulators as Saber, Eldo, Spectre-Verilog, Smash, *etc*.

For mixed signal systems with a digital part of high complexity, it seems more appropriate to describe the behavioral model (analog and digital) directly in VHDL and to synthesize the digital part using the required digital resources. In the digital domain, VHDL has proved its performances as a discrete simulation language devoted for discrete systems. In some attempts, VHDL has been used to describe some analog and mixed circuits but with limited success (Vachoux, 1998). Among the circuits which have been modelled with VHDL, we quote the sigma-delta analog-to-digital converter (Schubert, 2000; Baraniecki *et al*., 1998), the pipeline analog-to-digital converter (Peralias *et al*., 2000) and Multi-Slope A/D Converter (Maghrebi & Masmoudi, 2005).

With the growing trend of hardware designs that contain significant analogue and digital sections, comprehensive design environments that seamlessly integrate analogue and digital circuitry are necessary. Toward this end, the VHDL language (for which there are several design tools) was extended to support (in addition to digital) analogue and mixed-signal simulation. These extensions to VHDL have resulted in a new language called VHDL-AMS (Computer Society, 1997). In addition to the electrical domain, VHDL-AMS also supports mixed-domain modeling. Among the circuits which have been modelled and simulated whith VHDL-AMS (Zorzi *et al*., 2003; Hu *et al*., 2005; Szermer *e .al.,* 2003; Ewout *et al*., 2006)

The ADCs are precision products and their test usually requires high quality test equipment. With the advances of the ADCs, the required test equipment is becoming increasingly expensive. The test of the ADC linearity, i.e. integral nonlinearity (INL) and differential nonlinearity (DNL) typically constitutes the major portion of the test time (35-50%) and therefore the cost for testing ADCs (Cherubal & Chatterjee, 2000). Hence, we should provide the ADC structure test in the early steps of the design and specifically in the modeling phase.

In this paper, we introduce a programmable resolution analog-to-digital converter architecture modeling. This paper is organised as follow: Section two presents the various modules constituting the A/D converter. A static test ramp method is described in section three. Section four illustrates the ADC Simulation and behavioral modeling results using VHDL and the effect of the amplifier gain on the DNL and the INL of the converter. Section five gives the main conclusion of this work.

ADC STRUCTURE

Circuit description

In Figure 1, the block diagram of the analog to digital converter is illustrated. It consists of a reference voltage generator, a programmable gain amplifier, a low-resolution A/D converter (m bits) and the S/H block.

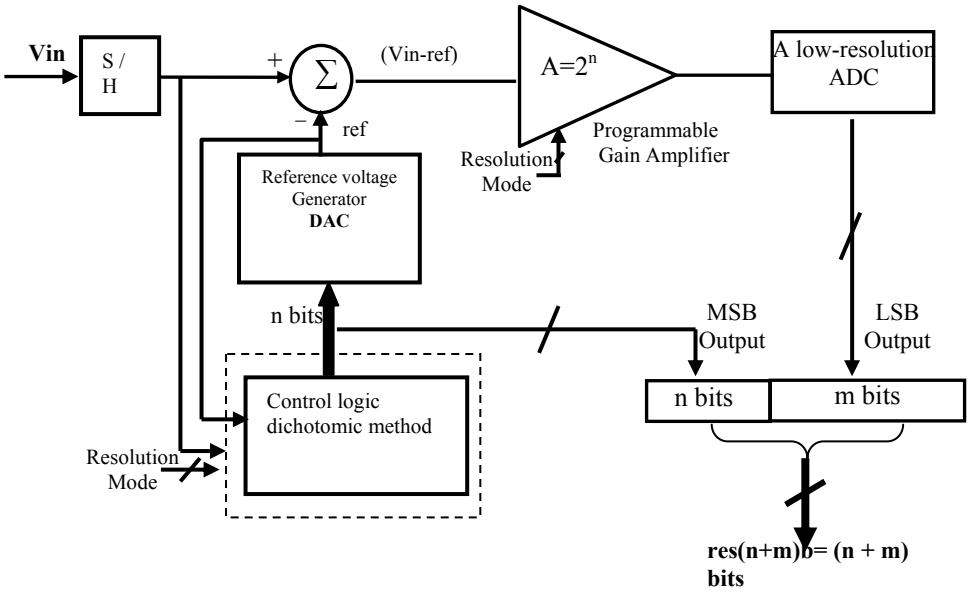

Figure 1. Bloc diagram of the A/D converter.

The dynamic input range is set to be [0, 2^n.Vref]. This scale is subdivided into 2^n intervals. To each interval corresponds only one code written in n bits (MSB). In the first step of the conversion algorithm, we should localize the interval to which belongs the analog input to be converted. This induces a quantization error. The second step of the conversion algorithm consists of evaluating this error. In fact, the obtained n-bits code is applied to a digital to analog converter whose output is subtracted from the analog input. The subtraction result (Vin-ref) is amplified using a programmable gain amplifier and then converted to an m-bits code (LSB).The whole digital result is written in (n+m) bits.

Dichotomic method

The reference voltage generator system should be reliable to provide stable voltages and to maintain less than 1 LSB as a commutation threshold. We have adopted the dichotomic method to localize the input voltage in the interval [0, 2^n.ref]. The number of steps to converge to a solution does not depend on the searched input value. This method is illustrated by the following algorithm (Figure 2):

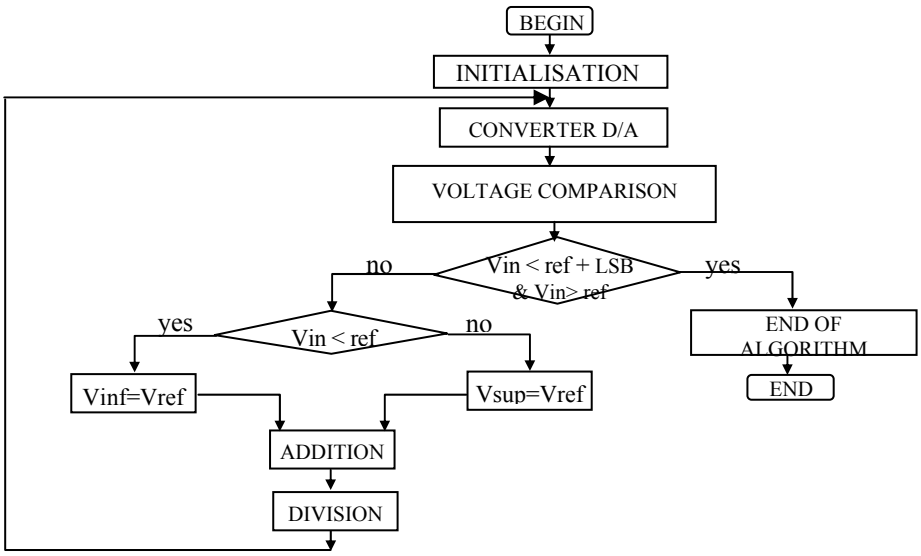

Figure 2. Dicothomic algorithm.

Vin is the input voltage, Vref is the reference voltage, which can take 2^n values. The dynamic range is set to be [Vinf, Vsup]. The conversion algorithm consists of many states. At the begining, the dichotomic algorithm startes by initializing the binary values of vinf, vsup and vref. The following state is to convert the binary output (vref) via the D/A converter to an analog value ***ref***. Then a step of comparison is used to compare the analog input value with two voltages, the reference value and the next reference value. The values Vinf and Vsup depend on Vref. If Vin is greater than ***ref***, the dynamic range becomes [Vref, Vsup]. In the other case, where Vin is less than ref, the dynamic range becomes [Vinf, Vref]. The new reference value to be used in the next loop of the algorithm is given by the expression Vref =Vinf +Vsup/2. The result is obtained after n loops. Therefore, the dichotomic method needs n steps to converge to the solution.

Dichotomic method with anticipation

To improve conversion, we propose the dichotomic method with anticipation. It consists of comparing the next input value to the previous ref and decide if it is necessary to recalculate the next Vref with dichotomic method. This method is illustrated by the following algorithm:

LSB= $FS/2^n$ // FS: the full scale
if (previous ref < next Vin < previous ref + LSB)Then
next Vref = previous Vref
Else
If (previous ref + LSB < next Vin) Then
dichotomic (previous Vref, Vsup) ;
else
dichotomic (Vinf, previous Vref) ;
End;

From this algorithm, we notice that the reference voltage Vref keeps the same value (next vref=previous vref) when the quantity (Vin–previous ref) is positive and less than LSB. In this particular case, the dichotomic method is not used. As a consequence, the circuit consumption will be reduced and the conversion speed will be increased. When the "next Vin" is less than "previous ref", or more than "previous ref" + LSB, the dynamic range will be [Vinf, previous Vref] and [previous Vref, Vsup], respectively. In this case, the dichotomic algorithm is begins. Consequently, the number of steps to converge to the solution is reduced.

Programmable resolution and gain values

Resolution programming allows the selection of 8 to 12 bits conversion. In this case, it is necessary to state precisely the input dynamic range for the chosen resolution. The dynamic range is determined by initializing Vinf, Vref and Vsup binary values. In the previous section, we note in the beginning of the dichotomic algorithm, that the initialization of these values depends on n. Therefore for each n value we can associate a resolution mode. There are five modes of resolution; we use three bits of selection ($S_1S_2S_3$) to decode these modes. Table 1 illustrates the initialization values for different resolution mode.

TABLE 1

Registers Binary Value Initialization

Resolution (m+n)	Mode ($S_1S_2S_3$)	registers binary value initialization		
		Vinf	Vsup	Vref
8 bits	000	inactif	inactif	Inactif
9 bits	001	00000	00010	00001
10 bits	010	00000	00100	00010
11 bits	011	00000	01000	00100
12 bits	100	00000	10000	01000

In addition to the initialization values, the amplifier gain should be fixed to 2^n. The programmable gain amplifier can be configured for voltage gains of 1, 2, 4, 8, and 16. A multiplexer is used to select a different gain for five resolution modes. The Amplifier Gain for each mode is given in Table 2.

TABLE 2

Amplifier Gain *vs* Resolution

Resolution (m+n)	n	Amplifier Gain
8 bits	0	1
9 bits	1	2
10 bits	2	4
11 bits	3	8
12 bits	4	16

.

It is noted that in Figure 1, the amplifier, the m-bits A/D converter and the reference generator are supposed to be ideal. The choice of ideal models is to validate the algorithm conversion.

STATIC TEST RAMP METHOD

The ramp method is one of the most classical techniques for ADC static test (Maghrebi & Masmoudi, 2003; Ben Smida *et al*., 2003). A digital-to-analog converter is used to generate the input analog signal as presented in Figure 3. Its input is incremented in very small step sizes.

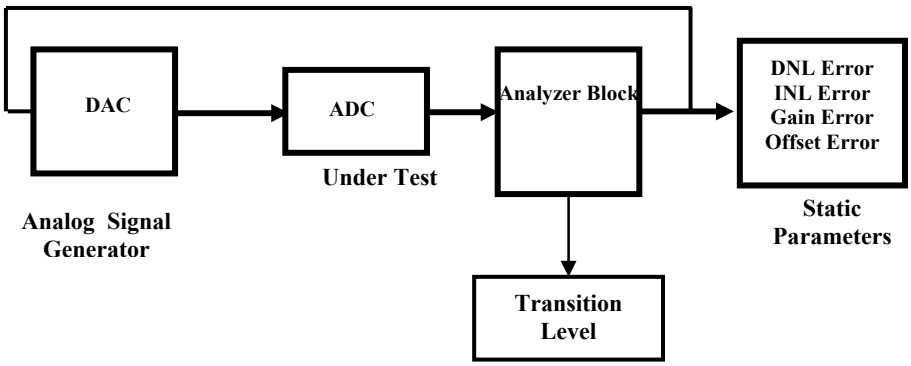

Figure 3. Static test ramp method.

At each step the ADC samples the DC level. This data is collected and analyzed by the analyzer block to determine the transition level of the code. As the analog is stepped through the transition region, the conversion results in a different distribution of output codes. When the converter under test converts the new code at least 50% of the time, the analog input voltage is recorded as the transition level for that code. This test uses the probabilistic definition of the transition level to determine their location. After determining the transition level location, specifications such as offset, gain, INL and DNL can be calculated. Also, monotonicity and amount of noise can be obtained.

RESULTS AND DISCUSSION

ADC simulation and behavioral modeling results

In Figure 1, we present the block diagram of the programmable resolution A/D converter. All parts have been modeled by using VHDL. The amplifier, the m-bits A/D converter and the reference generator are supposed to be ideal. Thus, the programmable resolution A/D converter model, in its first level, allows to validate the functionality of this circuit. Simulations of the 12-bits programmable resolution A/D converter are depicted in Figure 4 and Figure 5. Figure 4 illustrates simulation results obtained by using the dichotomic method. The conversion is initialized by taking the signal *smck* low. *Smck* is kept low until the sampling of the analog input *Vin*. The dichotomic algorithm starts by the rising edge of *Smck*.

Then the binary values of Vinf, Vsup and Vref are initialized, respectively at "*00000"*, "*10000"* and "*01000"*. Applying the dichotomic method, we can generate a higher 4 bits output (outn0_n3). This output is converted via the D/A converter to an analog value

ref. The subtraction result of *(Vin-ref)* is amplified by using a programmable gain amplifier. The amplifier output is then converted to an 8-bits word (outm0_m7). The desired digital output (results) is obtained from (outm0_m7+ outn0_n3).

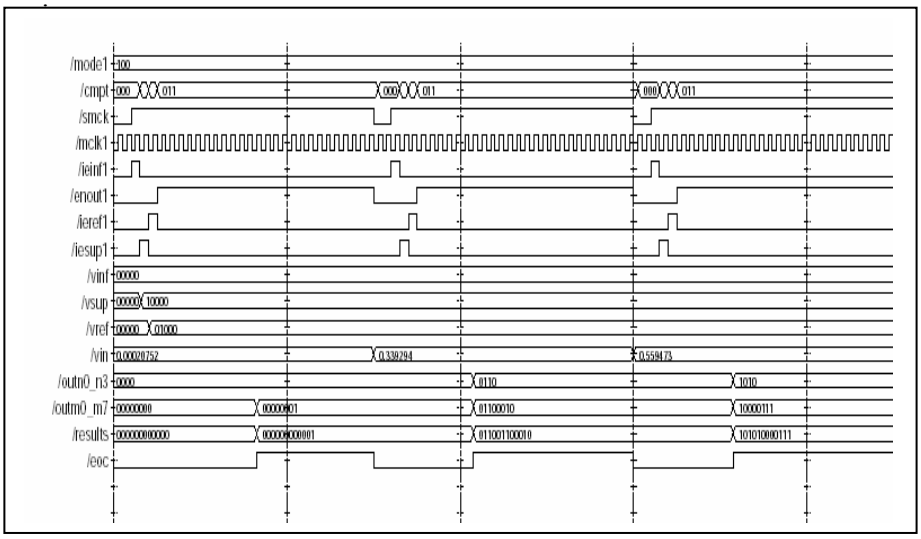

Figure 4. 12 bit A/D converter simulation results: dichotomic method.

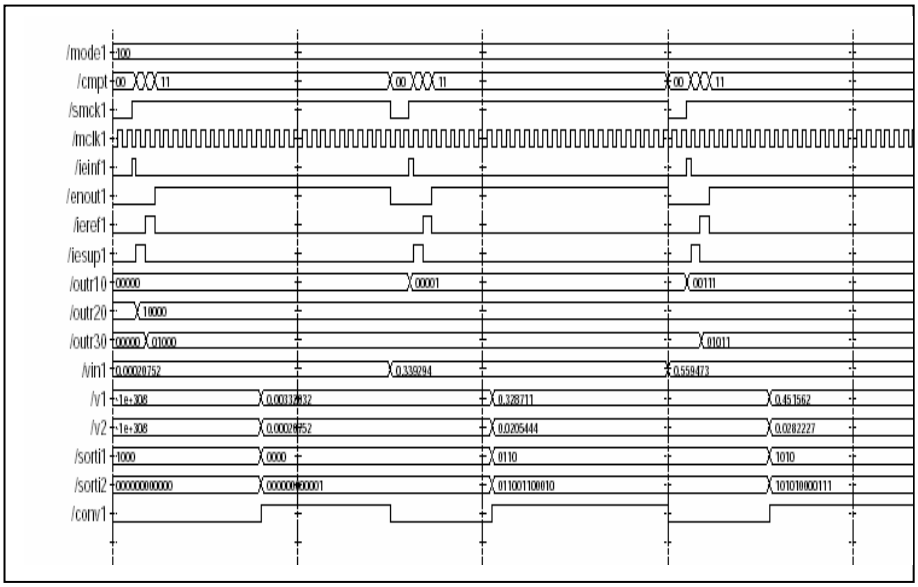

Figure 5. 12 bit A/D converter simulation results: dichotomic method with anticipation.

Dichotomic method with anticipation was applied to a 12-bit A/D converter to show the advantages of this method. The simulation results are shown in figure 5. We note, when next Vin is less than previous ref, or more than previous ref + LSB, the dynamic range will be [Vinf, previous Vref] and [previous Vref, Vsup], respectively, and the dichotomic algorithm starts with new binary registers values.

In Figure 6 (a) and (b), the INL and DNL errors given by VHDL simulation using voltage amplifier gain of 16 (12 bits) are shown. The maximum errors for DNL and INL are 0.0334 LSB and 0.0330 LSB, respectively.

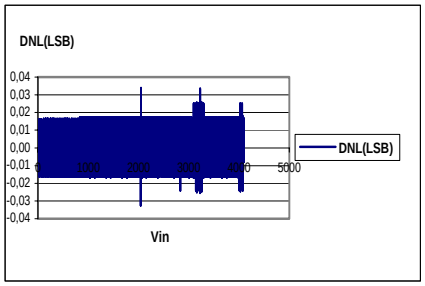

Figure 6a. 12 bit ADC: DNL error.

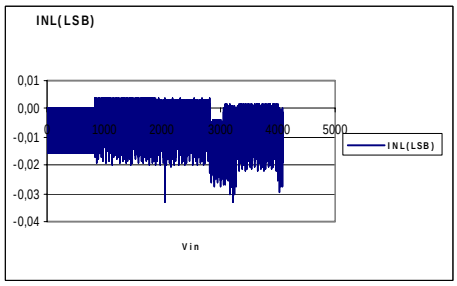

Figure 6b. 12 bit ADC: INL error.

Amplifier gain mismatch

The operational amplifier is a key component in most electronic circuits, including data converters. In fact, the performance of the operational amplifiers determines the performance of a complete data converter. It is therefore necessary to include an accurate model of the operational amplifiers, considering all non-ideal effects. In the previous section, we showed a 12-bits programmable resolution A/D converter simulation with ideal gain amplifier (A=16). The linearity of the A/D converter can be affected by a minor modification of the ideal voltage gain. This is illustrated in Figure 7 showing the maximum errors (for INL and DNL) obtained by varying the amplifier voltage gain. For a 6% voltage gain variation, the maximum errors for DNL and INL are ±0.8 LSB and ±0.55 LSB, respectively. However, for 9% voltage gain variation, the maximum errors for DNL and INL can be reached by ±1.1 LSB and ±0.65 LSB, respectively.

In this section, the results shown in Figures 7 and 8 illustrate the effect of amplifier non-idealities on overall converter performance. We notice that the converter architecture is sensitive to the variation of the amplifier gain. So, it will be necessary to allow a calibration of the amplifier after fabrication in order to avoid the deterioration of the converter performance.

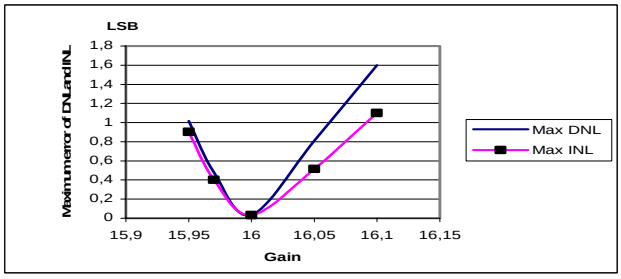

Figure 7. 12 bit ADC: DNL and INL errors.

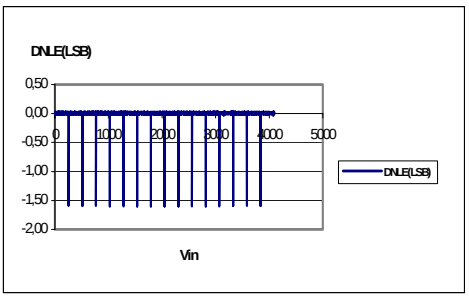

Figure 8 a. 12 bit ADC: DNL error.

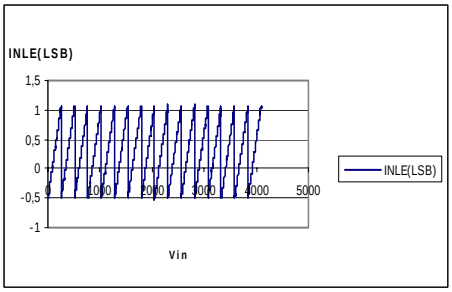

Figure 8 b. 12 bit ADC: INL error.

CONCLUSION

VHDL based models have been used to describe, simulate and verify programmable resolution A/D converter. The proposed conversion algorithm is based on the dichotomic method with anticipation which increases the conversion speed of the converter. The conversion algorithm has been validated by simulation results of the whole converter. A ramp technique has been used to determine the static parameters of the ADC under test. The converter structure can be affected by amplifier gain variation. We show while the variation of voltage gain does not exceed 9%, we obtain good result concerning for DNL and INL errors. As a consequence, it will be necessary to allow for a calibration of the amplifier after the fabrication process. The design of the programmable gain amplifier and the whole converter are an object of the forthcoming research.

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