EXPERIMENTAL RESULTS OF A FABRICATED ANALOG VLSI MULTIPLIER/TRANSCONDUCTANCE CIRCUIT

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ABSTRACT

In this paper, a fabricated analog VLSI Circuit is presented, which can be used as a four quadrant analog multiplier with high linearity on both terms of multiplication and wide range on one of them. These characteristics make the circuit useful for the implementation of a transconductance. The transconductance/multiplier can be used for general purpose in analog signal processing, but the circuit is suitable for Analog VLSI implementation of artificial neural networks because of its small silicon area and its low power consumption. The theoretical idea and the simulation by using Hspice are presented in (Chiblé, 2000), which is improved, fabricated and tested in this paper. The experimental results are presented.

Keywords: CMOS circuits, multiplier / transconductance, analog signal processing, VLSI, neural networks

INTRODUCTION

Analog VLSI Neural Networks (NN) are heavy parallel analog systems, which used and demonstrated in solving a wide range of real world problems (Annema, 1995). In this context, Analog Multipliers and Transconductances are key computational elements and they are very important to efficiently implement them; *e.g*. in a Multi Layer Perceptron MLP (Figure 1) each synapse needs a multiplier to multiply the input times the weight (Chiblé, 1997). The NN system may contain thousands of multipliers, because of that, the area and the power consumption must be as small as possible.

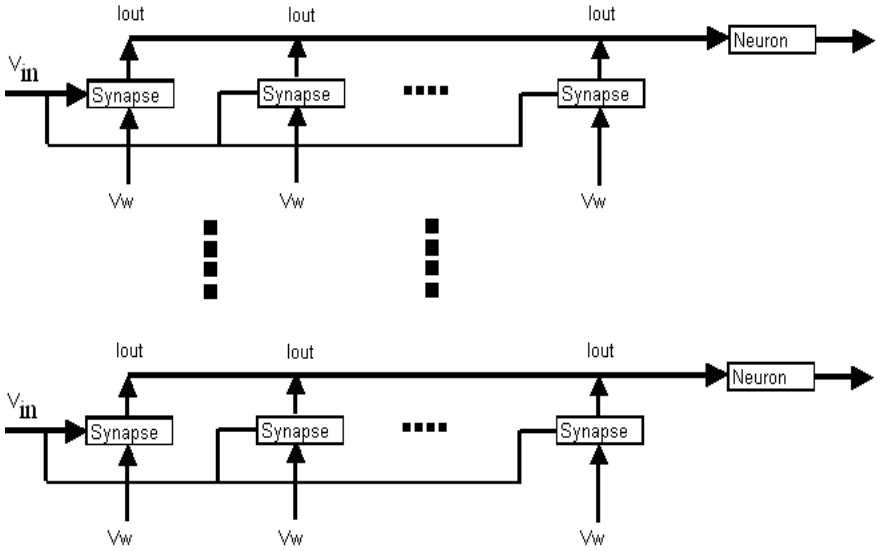


Figure 1. MLP network.

By definition the multiplier is used as a computational building block to multiply two input signals. While the transconductance is used to translate an input voltage into an output current. They can be used as a main element in analog signal processing systems such as filters, neural networks, mixers, and modulators.

In Valle *et al*., (1996) a non-linear multiplier with the following characteristics was proposed: 1) exponential relation between the output current and the weight voltage which varies in the range [0:5]V; 2) linear relation between the output current and the input voltage which varies in the range [2.4:2.6]V.

In Chiblé (1997) the multiplier proposed in (Valle *et al*., 1996) is modified in order to improve the learning of the neural networks. A quadratic relation instead of an exponential relation between the output current and the weight voltage is proposed.

In Chiblé (2000), the multiplier proposed in Chiblé (1997) is modified in order to achieve or to be near the ideal case, in which the NN can learn and work better. A linear relation instead of a quadratic relation between the output current and the weight voltage ([0:5] V) and a linear relation between the output current and the input voltage ([2.4:2.6]V) is proposed.

In this paper, the multiplier proposed in Chiblé (2000) is improved in three directions: 1) the circuit can be used as a Transconductance, in which it produces output current based on input voltage; 2) the supply voltage is decreased from 5V to 3.3V; 3) The circuit has been fabricated and tested. The experimental results are presented.

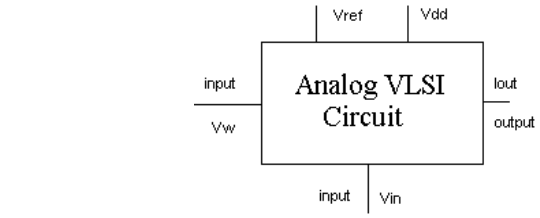
THE ANALOG VLSI CIRCUIT

Although high performance bipolar transistors multipliers have been available for some time, the CMOS multiplier implementation is still a challenging subject especially for low-voltage/low-power circuit design (Han and Sinencio, 1998). Weak-inversion is widely used in such circuits, but often it leads to low precision (Prodanov and Green, 1997). Multipliers for analog signal processing should have good linearity, wide range in at least one of the terms, in a small area (Annema, 1995). In the following a CMOS multiplier/transconductance circuit works in strong inversion (Strong inversion operation leads to small area and high precision) is presented. It combines from two stages: a square stage multiplied by a square root stage. It shows four quadrants operation, linearity, full range on one input and good insensitivity to variations in the technological process.

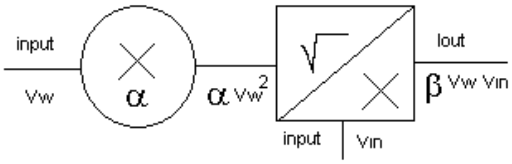
The analog VLSI circuit, as a black box, is shown in Figure 2 A. V_{dd} is the supply voltage (V_{dd} =3.3V), V_{ref} is the signal ground voltage (V_{ref}=1.65V), V_w is the first input voltage which is called the weight voltage V_w that varies in the range [0:3.3]V (V_w is positive if it varies in [1.65V:3.3V] else it is negative [0V:1.65V]), V_{in} is the second input voltage which varies in the range [1.6:1.7]V (V_{in} is positive if it varies in [1.65V:1.7V] else it is negative [1.6V:1.65V]), I_{out} is the result in current and it can take positive or negative values.

Figure 2B shows the circuit as a model of two boxes: the first is a box that produces the square of the input voltage Vw by a parameter α (α*Vw^2); the second is to take the square root of the output of the first box and multiply it by another input voltage Vin and it produces βVwVin.

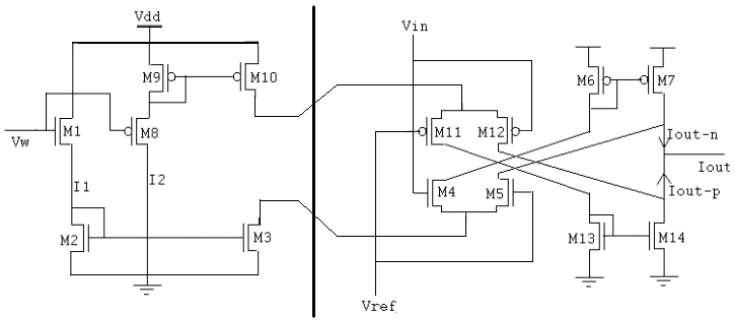
Figure 3C shows the transistor level circuit: the first part represents the box that produces α*Vw^2 [M1, M2, M3, M8, M9, M10]; the second part represents the box that produces βVwVin [M4, M5, M6, M7, M11, M12, M13, M14]. It is explained in detail in (Chiblé, 2000). If V_w=V_{ref}=1.65V then I_{out} =0 and if V_{in}=V_{ref}=1.65V then I_{out} =0. V_w (or V_{in}) is considered positive value if it is greater than V_{ref}, else it is negative one. This circuit can be considered as a multiplier and as a transconductance. See the next sections for equations.



(A)



(B)



(C)

Figure 2. The Analog VLSI Circuit as a black box (A); as a model of boxes (B); as CMOS circuit (C).

THE MULTIPLIER EQUATIONS

The output current I_{out-n} is given by (Chiblé, 2000):

$$I_{out-n} = \sqrt{\frac{\beta_n \beta_{5,4}}{2n^2}}\left(V_w - nV_{TH2} - V_{TH1}\right)\left(V_{in} - V_{ref}\right)$$

where $ß_n$ is given by:

$$\frac{1}{\sqrt{\beta_n}} = \frac{1}{\sqrt{\beta_1}} + n\frac{1}{\sqrt{\beta_2}}$$

$ß_1$, $ß_2$, $ß_4$, $ß_5$ are respectively the transfer parameter of transistors M1, M2, M4 & M5 ($ß_{5,4}$=$ß_5$=$ß_4$).

The output current I_{out-p} is given by Chiblé (2000):

$$I_{out-p} = \sqrt{\frac{\beta_p \beta_{11,12}}{2n^2}}\left(V_w - n^2 V_{dd} + nV_{TH9} + V_{TH8}\right)\left(V_{ref} - V_{in}\right)$$

where $ß_p$ is given by:

$$\frac{1}{\sqrt{\beta_p}} = \frac{1}{\sqrt{\beta_8}} + n\frac{1}{\sqrt{\beta_9}}$$

$ß_8$, $ß_9$, $ß_{11}$, $ß_{12}$ are respectively the transfer parameter of transistors M8, M9, M11 & M12 ($ß_{11,12}$=$ß_{11}$=$ß_{12}$).

The value $ß_1$ is given by $\beta_1 = \mu_1 \times C_{ox}\left(W/L\right)_1$: where n is the slope factor usually smaller than 2 which tends to 1 for very large values of the gate voltage (Vittoz, 1994), μ_1 is the carrier mobility of the transistor M_1, C_{ox} is the gate oxide capacitor per unit area, $(W/L)_1$ is the channel width-to-length ratio of M_1, V_{TH1} is the gate threshold voltage of M_1, V_1 is the source voltage of M_1. The same for $ß_2$, $ß_4$, $ß_5$, $ß_8$, $ß_9$, $ß_{11}$ and $ß_{12}$.

The output current of the four-quadrant multiplier I_{out} is given by:

$$I_{out} = \begin{cases} I_{out-n} \ldots\ldots If \ldots 1.65V < Vw < 3.3V \\ I_{out-p} \ldots\ldots If \ldots 0V < Vw < 1.65V \end{cases}$$

$$I_{out} = \begin{cases} \sqrt{\frac{\beta_n \beta_{5,4}}{2n^2}}\left(V_w - nV_{TH2} - V_{TH1}\right)\left(V_{in} - V_{ref}\right) \ldots\ldots If \ldots 1.65V < Vw < 3.3V \\ \sqrt{\frac{\beta_p \beta_{11,12}}{2n^2}}\left(V_w - n^2 V_{dd} + nV_{TH9} + V_{TH8}\right)\left(V_{ref} - V_{in}\right) \ldots\ldots If \ldots 0V < Vw < 1.65V \end{cases}$$

Note 1: The output current I_{out} does not have exact linear relation when Vw near 1.65V, this because the transistors (M4, M5, M11, M12) work in moderate inversion and not exactly in strong inversion (Chiblé, 2000). While vice versa (it is linear) when Vw far 1.65V (Figure 6). This effect is clearly shown in the correspondence Transconductance figure (Figure).

Note 2: The output current I_{out} is equal to the output current I_{out-p} if the weight is negative (0V < Vw < 1.65V) (*i.e.* the output current of the I_{out-n} is equal to 0), and vice versa, when

the weight is positive (1.65V <Vw <3.3V), $I_{out} = I_{out\text{-}n}$ (i.e. $I_{out\text{-}p=0}$). While the sign of the $I_{out\text{-}p}$ & $I_{out\text{-}n}$ is determined by the value of V_{in} as follows:

$$I_{out-n} = \begin{cases} Positive\ldots\ldots If\ldots 1.65V < Vin < 1.7V \\ Negative\ldots\ldots If\ldots 1.6V < Vin < 1.65V \end{cases}$$

$$I_{out-p} = \begin{cases} Negative\ldots\ldots If\ldots 1.65V < Vin < 1.7V \\ Positive\ldots\ldots If\ldots 1.6V < Vin < 1.65V \end{cases}$$

THE TRANSCONDUCTANCE EQUATIONS

The same circuit can be considered as a transconductance because it produces an output current based on input voltage. We have two types of transconductance:

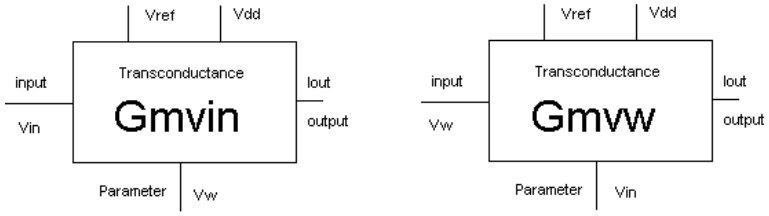


Figure 3. Gmvw & Gmvin transconductances.

(1) Gmvin is obtained if the input voltage is Vin, while Vw is a parameter. Gmvin-n can be obtained by doing the derivative of the equation of Iout-n with respect to Vin as shown in the following equation:

$$G_{mvin-n} = \frac{dI_{out-n}}{dV_{in}} = \sqrt{\frac{\beta_n \beta_{5,4}}{2n^2}}\left(V_w - nV_{TH2} - V_{TH1}\right)$$

It is constant with respect to Vin. But its value can be controlled by the parameter Vw.

The same for Gmvin-p, which is given by:

$$G_{mvin-p} = \frac{dI_{out-p}}{dV_{in}} = -\sqrt{\frac{\beta_p \beta_{11,12}}{2n^2}}\left(V_w - n^2 V_{dd} + nV_{TH9} + V_{TH8}\right)$$

Gmvin is given by:

$$G_{mvin} = \begin{cases} G_{mvin-n} \ldots\ldots If \ldots 1.65V < Vw < 3.3V \\ G_{mvin-p} \ldots\ldots If \ldots 0V < Vw < 1.65V \end{cases}$$

$$G_{mvin} = \begin{cases} \sqrt{\frac{\beta_n \beta_{5,4}}{2n^2}} \left(V_w - nV_{TH2} - V_{TH1}\right) \ldots\ldots If \ldots 1.65V < Vw < 3.3V \\ -\sqrt{\frac{\beta_p \beta_{11,12}}{2n^2}} \left(V_w - n^2 V_{dd} + nV_{TH9} + V_{TH8}\right) \ldots\ldots If \ldots 0V < Vw < 1.65V \end{cases}$$

$$G_{mvin} = f(V_w, \beta_n, \beta_p, \beta_{5,4}, \beta_{11,12}, n, V_{TH1}, V_{TH2}, V_{TH8}, V_{TH9})$$

(2) Gmvw is obtained if the input voltage is Vw, while Vin is a parameter. Gmvw-n can be obtained by doing the derivative of the equation of Iout-n with respect to Vw as shown in the following equation:

$$G_{mvw-n} = \frac{dI_{out-n}}{dV_w} = \sqrt{\frac{\beta_n \beta_{5,4}}{2n^2}} \left(V_{in} - V_{ref}\right)$$

It is constant with respect to Vw. But its value can be controlled by the parameter Vin.

The same for Gmvw-p, which is given by:

$$G_{mvw-p} = \frac{dI_{out-p}}{dV_w} = \sqrt{\frac{\beta_p \beta_{11,12}}{2n^2}} \left(V_{ref} - V_{in}\right)$$

Gmvw is given by:

$$G_{mvw} = \begin{cases} G_{mvw-n} \ldots\ldots If \ldots 1.65V < Vw < 3.3V \\ G_{mvw-p} \ldots\ldots If \ldots 0V < Vw < 1.65V \end{cases}$$

$$G_{mvw} = \begin{cases} \sqrt{\frac{\beta_n \beta_{5,4}}{2n^2}} \left(V_{in} - V_{ref}\right) \ldots\ldots If \ldots 1.65V < Vw < 3.3V \\ \sqrt{\frac{\beta_p \beta_{11,12}}{2n^2}} \left(V_{ref} - V_{in}\right) \ldots\ldots If \ldots 0V < Vw < 1.65V \end{cases}$$

$$G_{mvw} = f(V_{in}, V_{ref}, \beta_n, \beta_p, \beta_{5,4}, \beta_{11,12}, n)$$

THE FABRICATED CHIP OF THE CIRCUIT

The Analog VLSI Circuit has been designed and simulated by using the technology ES2 CMOS 0.7 μm (ECPD07 process) with double metal layers and only one level of polysilicon (Chiblé, 2000). It is redesigned & fabricated with the parameters of the Alcatel-Mietec technology CMOS 0.5, which is used for analog implementation. The width and the length of the MOS transistor have been computed on the base of the technology parameters (*e.g*. the mobility of the electron, oxide capacitor, *etc*.).

The following procedure is used to design and prepare the circuit layout to be fabricated:

1. Design the width and length of each transistor in Figure 2C;
2. Simulate the circuit - by using the Hspice simulator software - to obtain the required results;
3. Create the physical layout;
4. Create the description – by using Cadence software– to simulate the layout;
5. Simulate the layout - by using the Hspice simulator - to see if the required results are obtained;
6. If the required results are obtained, then fabricate (as shown in Figure 4). Else redesign the circuit in Figure 2C.

After the last step (fabrication of chip), we have to measure the chip, and the results obtained in simulation are expected. In this paper, we present the measurement results, and by comparing the simulation results and the measurements results obtained in the next section, we see the effectiveness of the above method.

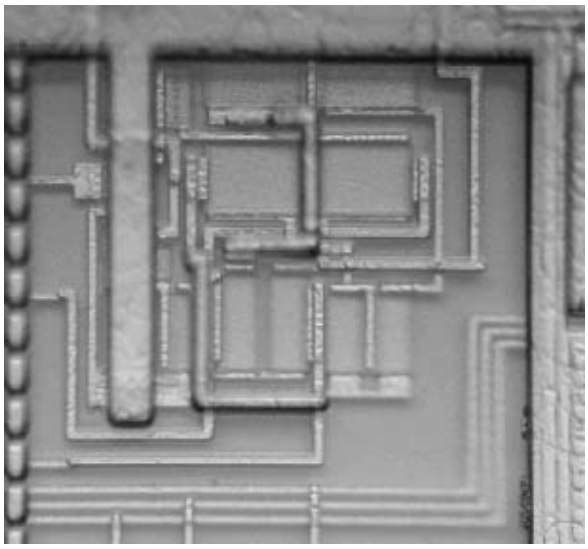


Figure 4. An actual photo of the physical layout of the analog VLSI circuit in the fabricated chip.

After applying the above procedure, the aspect ratio (width/length) of the transistors are obtained as follows: M_1, M_2, M_3, M_4, M_5, M_6, M_7, M_8, M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14} are respectively equal to 2/20, 8/12.5, 2/12.5, 5/15.5, 5/15.5, 15/12.5, 15/12.5, 6/5, 8/10, 2/10, 15/11.5, 15/11.5, 5/12.5, 5/12.5. The length and the width are measured by the micrometer (μm) unit. The total silicon area of the multiplier is computed from the physical layout, which is approximately equal to 60*60μm^2, it was 70*70μm^2 in (Chible, 2000).

REAL MEASUREMENT RESULTS

After fabricating the circuit, the main question is to test and measure the characteristics of the circuit. First thing is to propose a system to do that.

Figure 5 shows the system proposed. It is an HP4155 logic state analyser.

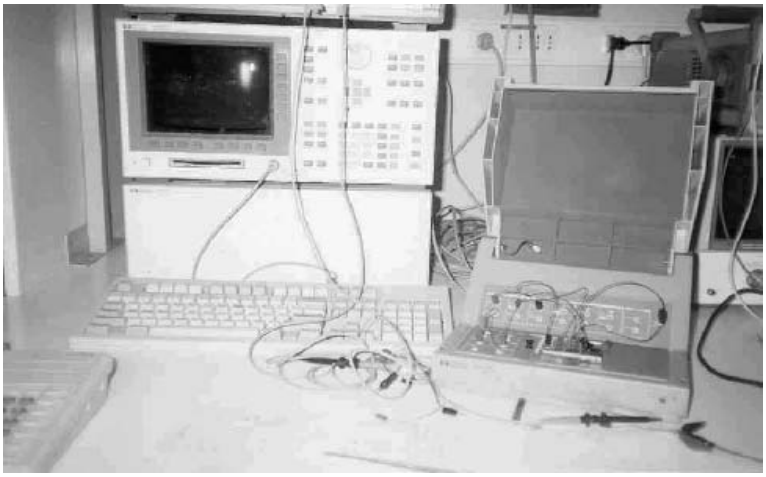


Figure 5. The logic state analyser system to test and measure the circuit.

The power consumption tested is approximately equal to 14μw, it was 15μw in (Chiblé, 2000). Actual measurement results are presented as follows:

1. **The output current Iout versus the input voltage Vin & versus the weight voltage Vw**

Figure 6 shows the relation between the output current Iout and the input voltage Vw for several Vin changing uniformly from 1.6V to 1. 7V. Figure 7 shows the relationship between the output current Iout and the input voltage Vin for several Vw changing uniformly from OV to 3.3V. Figure 6 & Figure 7 show the output current Iout which varies in the range [-400:400] nA. The minimum output current Iout=-400nA is obtained if Vin=1.6V & Vw=3.3V or if Vin=1.7V & Vw=0V. The maximum output current Iout=+400nA is obtained if Vin=1.6V & Vw=0V or if Vin=1.7V & Vw=3.3V. Iout=0 if Vin or Vw equals to 1.65V.

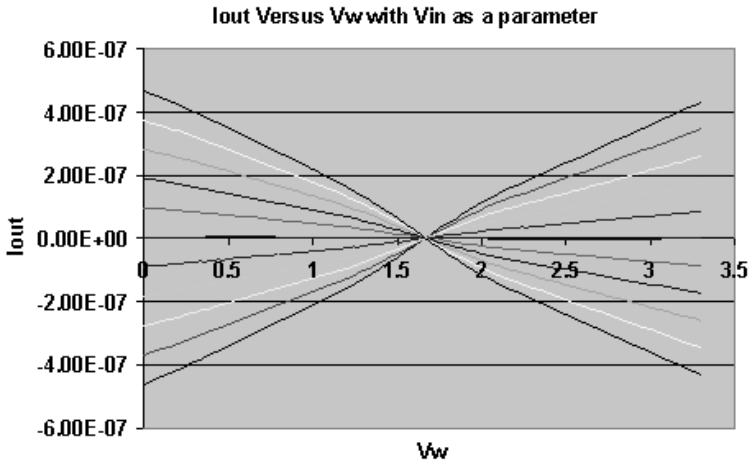


Figure 6. Iout versus Vw (which varies between 0:3.3 with step 0.05) with Vin as a parameter (which varies from 1.6V to 1.7V with step 0.01V).

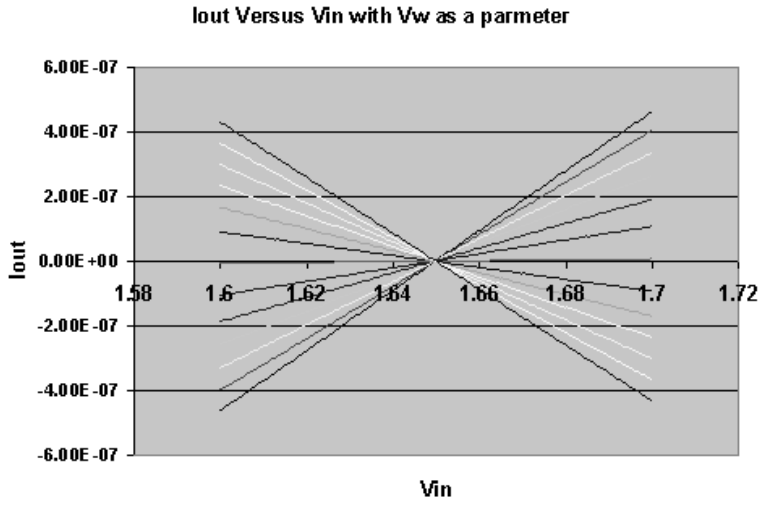


Figure 7. Iout versus Vin (which varies between 1.6V:1.7V with step 0.001V) with Vw as a parameter (which varies from 0V to 3.3V with step 0.275V).

2. The transconductance Gmvin versus the input voltage Vin & Gmvw versus the input voltage Vw

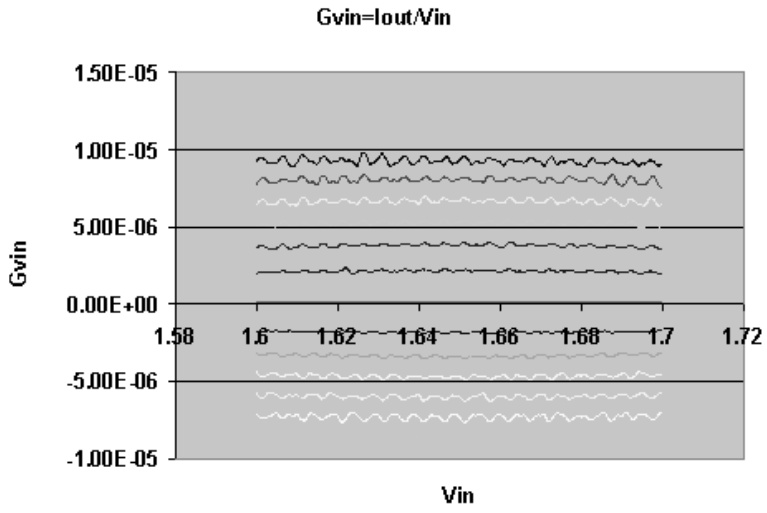


Figure 8. Gmvin versus Vin (which varies between 1.6V:1.7V with step 0.001V) with Vw as a parameter (which varies from 0V to 3.3V with step 0.275V).

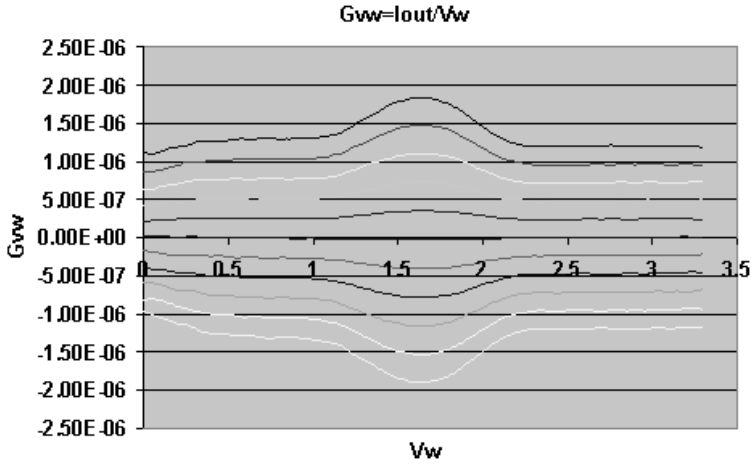


Figure 9. Gmvw versus Vw (which varies between 0:3.3 with step 0.05) with Vin as a parameter (which varies from 1.6V to 1.7V with step 0.01V).

3. Comparison between four chips: Iout versus Vin & versus Vw

This comparison is tested to see the variation on different chips. The following two figures shows clearly that the effect variation is negligible.

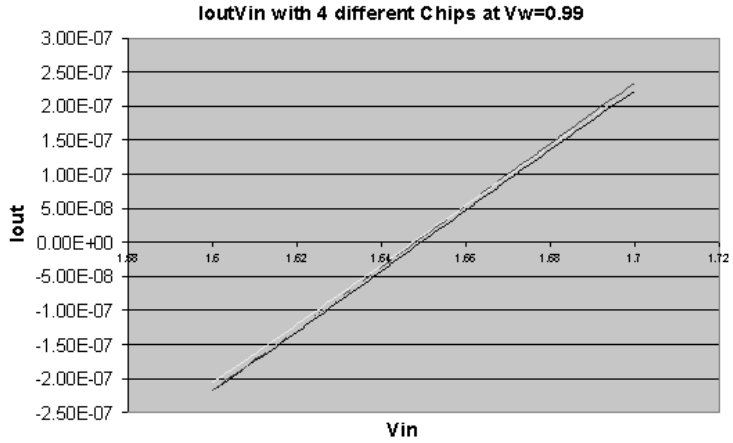


Figure 10. Iout versus Vin (which varies between 1.6V:1.7V with step 0.001V) with Vw as a constant parameter equals to 0.99V for four different chips.

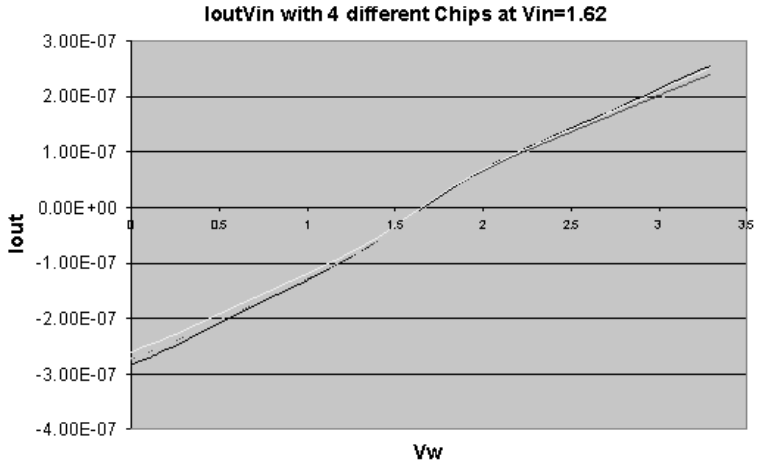


Figure 11. Iout versus Vw (which varies between 0:3.3V with step 0.05V) with Vin as a constant parameter equals to 1.62V for the same four different chips used to produce Figure 10.

CONCLUSIONS

The circuit presented cannot be classified in the standard families of multipliers (Han and Sinencio, 1998). This circuit can be used as a basic element in analog signal processing. It shows wider range (Vdd) for one of the input and limited on the other. For this aspect and its high linearity, this circuit is useful for the implementation of transconductors and for synapses (multiplier to multiply the weight voltage by the information input voltage and to produce an output current) in artificial neural networks. A good insensitivity from the statistical variation of the parameters of the technological process is shown. In neural network applications, in which feedback loops take into account errors, this variation should be furthermore reduced (Bo *et al*., 1999). The silicon area used is about 60 x 60μm^2 and the power consumption is 14μW.

ACKNOWLEDGEMENTS

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